STRATEGIES TOWARDS THE MITIGATION OF SHUNTING IN IMPLANTED NEURAL ARRAYS TO IMPROVE DEVICE STABILITY FOR CHRONIC APPLICATIONS

by

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STATEMENT OF DISSERTATION APPROVAL

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ABSTRACT

By enabling neuroprosthetic technologies, neural microelectrodes can greatly improve diagnostic and treatment options for millions of individuals living with limb loss, paralysis, and sensory and autonomic neural disorders. However, clinical use of these devices is restricted by the limited functional lifetimes of implanted electrodes, which are commonly less than a few years. One cause is the evolution of damage to dielectric encapsulation that insulates microelectrodes from the physiological environment. Fluid penetration and exposure to an aggressive immunological response over time may weaken encapsulating films and cause electrical shunting. This reduces electrode impedance, diverts electrical signal away from target tissue, and causes multi-channel crosstalk. To date, no neural microelectrode encapsulating material or design approach has reliably resolved this issue. We employ the parylene C-encapsulated Utah Electrode Array (UEA), a silicon-micromachined neural interface FDA-cleared for human use, to execute three aims that address this challenge through investigations of new materials, electrode designs, and testing methods.

We first evaluate a novel bilayer encapsulating film comprised of atomic layer deposited Al_2O_3 and parylene C, testing this film using UEAs and devices with UEA-relevant topography. Contrasting with previous work employing simplified planar structures, the incorporation of neural electrode features on test structures revealed failure modes pointing to the dissolution of Al_2O_3 over time. Our results emphasize the need for

dielectric coatings resistant to water degradation as well as test methods that take electrode features into account. In our second aim, we show through finite element modeling and aggressive *in vitro* testing that use of degenerately doped silicon as a conductive neural electrode material can mitigate the consequences of encapsulation damage, owing to the high electrochemical impedance of silicon. Our final aim compares oxidative *in vitro* aging to long-term *in vivo* material damages and finds clear evidence that such *in vitro* testbeds may help predict certain *in vivo* damage modes. By pairing this testing with absorption and emission spectroscopic characterization modalities, we identify contributors to material damage and future design solutions. Our results will inform future material and testing choices, to improve the resilience of neural electrode dielectric encapsulation and enhance the longevity of neuroprostheses.

For Eden.
You're welcome.

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CHAPTER 1

INTRODUCTION

Implantable neural microelectrodes enable direct interfacing between neurons and machines, enabling exciting technologies such as neuroprosthetics for individuals with paralysis and limb loss. However, the functional lifetime of these devices is not sufficiently long for clinical adoption of these technologies. Device failures can be attributed to a number of factors involving both biological processes and material degradation. The current work advances existing knowledge by addressing how dielectric material function on neural interfaces can be tested and improved to reduce electrical shunting of electrodes, which is an acknowledged failure mode for implantable neural arrays. This chapter introduces the reader to microelectrode neural interfaces for neuroprosthetics, including how they differ from interfaces used clinically as well as their failure modes, material construction, and techniques for characterization and testing. Three approaches are then described to address challenges in dielectric performance for microelectrodes and advance neural electrode state-of-the-art.

1.1 Background of neural interfaces

As the irreplaceable organ system responsible for the human experience, the human nervous system must function properly for the best quality of life. The complexity

of this system is reflected in the many pathologies that can affect its function, which may originate through genetic, traumatic, disease, or environmental mechanisms. The World Health Organization has estimated that one out of every seven people lives with symptoms or effects of neurological disorders, and has projected that by 2030, such disorders will comprise 7% of the global health burden [1]. An exciting and relatively new treatment option for these disorders utilizes the electrical characteristics of neural tissue to treat neural disorders, the discovery of which is attributed to Luigi Galvani in his 1791 publication *De Viribus Electricitatis in Motu Musculari*. Neural interfaces are medical devices that take advantage of the electrical excitability of neurons by connecting neural tissue with electronic hardware, facilitating charge transfer between biology and electronics. These devices can decode, stimulate, and modulate neural signals, to improve the quality of life for individuals afflicted with neurological impairments [2]–[5].

Neural interface structure is driven by function, and the needs that neural interfaces meet include functions relating to diagnostics, brain activity modulation, sensory/motor restoration, and treatment of several diseases. Utilizing electroencephalography (EEG), a noninvasive technique whereby neural signals are detected by an electrode grid in intimate contact with the scalp, diagnoses can be made concerning sleep disorders, coma, and seizures [6]–[8]. Mapping of seizure foci for surgical treatment can be done with higher fidelity using electrocorticography (ECoG), in which an electrode grid is placed on surgically exposed cortex [9]. ECoG can also play a role in cortical stimulation mapping, which identifies eloquent cortical regions through direct electrical stimulation and response detection, to avoid damaging functional tissue during surgical resection procedures such as epilepsy treatment [10].

In cases where surgical resection is not a treatment option for refractory epilepsy, neuromodulation may be considered [11]. Vagal nerve stimulation (VNS) is an established neuromodulation therapy for epilepsy [12], whereby electrodes stimulate the vagus nerve to influence autonomic neural behavior and inhibit the synchronized neural activity that drives seizures. Deep brain stimulation is another example of a neuromodulation treatment, which is marketed to reduce tremors from Parkinson's disease and treat depression [13]–[17], and being evaluated for the treatment of pain. In contrast to many neural interfaces used for diagnoses that are operated by medical professionals, neuromodulation devices are designed to treat diseases outside the clinic environment. Stimulation pulses are controlled through an implanted pulse generator (IPG) connected to electrodes that are left to reside chronically in the target tissue, which may be the spinal cord, peripheral nerves such as the vagus and trigeminal nerves, or deep brain nuclei [18]–[20]. Such systems are designated by implant location, such as spinal cord stimulation (SCS), vagus or trigeminal nerve stimulation (VNS or TNS), or deep brain stimulation (DBS), respectively. Electrodes for SCS and DBS may be cylindrical with a high aspect ratio for insertion into tissue, or they may be cuff-like to wrap around nerves for VNS and TNS.

Implanted neural electrodes can also be employed to restore sensory or motor function, a field known as neuroprosthetics [3], [21], [22]. The cochlear implant is a well-known neuroprosthetic device, which stimulates the cochlear nerve in response to sound in order to improve sound perception for appropriate severely and profoundly deaf patients [23]. The restoration of sight through direct stimulation of retinal ganglion cells or the visual cortex [24]–[26] is also of great interest, with one marketed retinal

prosthesis system [27]. Rather than IPGs used for neuromodulation, cochlear and retinal implants incorporate processors that convert sensor input into electrical pulse patterns, which stimulate neurons in a manner that provides useful sensory restoration. The neural electrodes themselves must also accommodate a higher spatial resolution than existing neuromodulation electrodes, and thus have finer electrode architectures. For example, typical DBS electrodes are cylindrical with electrode diameter, height, and pitch greater than 1 mm [28]. In contrast, electrodes for cochlear and retinal implants are circular with diameter and pitch much less than 1 mm [26], [29]. This smaller size permits electrode-tissue interactions suitable for fine sensory resolution, through voltage pulsing to induce neuronal stimulation. In addition to high-resolution stimulation, micrometer-scale electrodes (microelectrodes) can resolve the extracellular action potentials of individual neurons, as compared to the low spatial resolution of recordings using EEG and even ECoG [30], [31]. Due to the ability to record and stimulate down to the single-neuron-level, microelectrode neural interfaces are an exciting technology with the potential to revolutionize treatment for individuals with sensory and motor impairments, such as paralysis and a number of other conditions.

1.2 Microelectrodes: motivation and challenges

It is estimated that approximately 6 million people are living with paralysis, and the lifetime cost of living for a single paralyzed individual can surpass $3 million [32]. Restoring independence to these individuals will not only greatly improve their quality of life, but can also reduce the cost of care. Sensorimotor neuroprosthetics are an example of the promise held by these technologies, as they can respond to intact neural commands in

order to drive motor behavior and sensory feedback in a way that bypasses non-functional afferent and efferent pathways [3], [22], [33], [34]. Individuals with amputated limbs can also benefit from neuroprosthetics that interface with spared nerves to allow the patient to embody a prosthetic limb [35]–[38]. These technologies rely heavily on implantable microelectrode interfaces that can create high-fidelity communication pathways between neural tissue and electronics. Penetrating microelectrodes that are directly inserted into the cortex or peripheral nerves have the benefits of high selectivity and sensitivity [21], [39]–[42], but are also more invasive. Unfortunately, the functional lifetime of implanted penetrating microelectrodes is typically on the order of months [43], and reliable operation *in vivo* for over 10 years is widely regarded as a benchmark for clinical acceptance [44]. Both biotic and abiotic failure modes contribute to the challenges that must be addressed in order for the full benefits of implantable microelectrodes to be realized. The peri-implant environment plays an important role in both types of failure modes, and while this work focuses on addressing abiotic failure modes, biotic mechanisms are presented for completion and context.

1.2.1 Biotic degradation mechanisms

One mode of electrode failure arises from degradation of the biological environment itself. This is a more considerable challenge to microelectrode performance than to the performance of larger macroelectrodes in clinical use, due to the smaller scale of microelectrodes, which are designed for higher selectivity. To attain a spatiotemporal resolution sufficient for the highest fidelity performance of cortical neuroprosthetic applications, it has been reported that the microelectrode site must be within 140 µm of a

viable neuron [45]. Penetrating microelectrodes can routinely be within this distance, but the tissue injury sustained from implantation prompts an inflammatory foreign body response (FBR) [46], [47]. The harsh ionic physiological environment [48], [49] may become more harsh during the FBR through activation of a number of pathways, which can shorten the microelectrode performance lifetime. These include migration and activation of immune cells [50], [51] that release of inflammatory cytokines and reactive oxygen species (ROS) [52], [53]. As a result, neuronal cell loss in the target region is sustained [54], [55], and the shank is encapsulated by a non-neuronal tissue sheath [56], [57]. These factors combine to increase the effective distance between electrode site and viable neurons, reducing microelectrode recording sensitivity to extracellular signals [58]. Stimulation paradigms may also become less effective, with increases to stimulation current necessary to evoke neuronal responses [35], [59].

Interestingly, recent work has found FBR intensity to be inversely proportional to size for implant diameters up to 1.5 mm [60], which may work to the benefit of DBS implants and similar, but may increase the challenge of reducing the microelectrode FBR. However, other groups have noted reduced FBR for electrodes of extremely small surface area, [61], [62], thus solutions to resolving the FBR may be present at both extremes. Considerable efforts are underway to mitigate the tissue response to neural microelectrodes, through informed design of microelectrode geometry [63], materials [64], [65], and chemical/biological treatments [66]–[68]. Through such advancements, tissue health at the implant site may be maintained to ensure intimate contact between electrodes and viable neurons over the long term. However, the effectiveness of these solutions is limited if the electrode itself sustains damage that impacts performance.

Abiotic damage modes must also be addressed in order to improve long-term reliability of neural microelectrodes.

1.2.2 Abiotic degradation mechanisms

The physiological environment, potentially exacerbated by FBR conditions, can also damage neural electrode materials, contributing to abiotic electrode failures. The ionic physiological environment is already hostile to electrical devices, and the addition of immunological factors such as ROS may exacerbate electrode decline. **Numerous studies have observed damage to implanted microelectrode materials** [26], [69]–[76]**, making apparent the need for electrode materials and designs that deliver stable performance in the physiological environment**. These materials include those used for tissue/electrode charge transfer as well as dielectric encapsulation, and mitigation of failures associated with the latter is the primary subject of the present work. The interconnection mechanism between implanted electrodes and external hardware has also been acknowledged as a significant failure point, as it is commonly made with wiring that passes through skin, and carries risks of infection as well as wire breakage [72], [77]. A wireless telemetry solution is widely regarded as a necessary next step to mitigate these risks, and the development of low-power wireless interconnect technologies for neural interfaces is well underway [78]–[83]. However, performance of the neural electrode interconnect is not a focus of the work and so it is omitted from further discussion, which will focus on microelectrode architectures and characterization techniques.

1.3 Microelectrode architectures and materials

The general architecture of penetrating microelectrodes is well conserved among different styles. Devices are built from a substrate with a sharp tip and high aspect ratio for penetrating up to 1 mm or more into neural tissue. At the penetrating tip or along the length of the substrate are exposed electrode sites through which charge flows between device and tissue. Conductive paths connect to these sites and traverse along the substrate length to an interconnect site, enabling current flow between the interconnect and electrodes. These conductive paths are insulated from the physiological environment by dielectric encapsulation. The subsections that follow describe in more detail the types of materials used for each aspect of the general microelectrode, as well as common microelectrode designs currently used for *in vivo* animal and human trials.

1.3.1 Electrode site materials

In order for charge to flow between electronic hardware and biological tissue, it must be converted from electron current to ionic current. This conversion can occur at the electrode site through capacitive and faradaic mechanisms [42], and the resistance to charge flow through an electrode site into the *in vitro* or *in vivo* environment is measured through impedance spectroscopy, to be discussed in a later section.

Capacitive mechanisms rely entirely on the electrical double layer capacitance of the electrode. Any charged surface immersed in ionic solution is known to be coated by an electrical double layer of charged particles [84], and a change in voltage at the surface will alter surface charge and cause rearrangement of these charged particles, resulting in ionic current. Purely capacitive charge transfer does not generate chemical byproducts

and is thus generally viewed as the safer of the two mechanisms, but the impedance associated with capacitive mechanisms is typically higher than faradaic mechanisms. Faradaic materials participate in electron-transfer reactions between electrode and electrolyte, facilitating lower impedances but also generating oxidized or reduced byproducts. The risk of damage due to these byproducts is generally only notable during current stimulation applications, and use of charge-balanced stimulation pulses is generally encouraged to facilitate zero net byproducts [85]–[88]. Many electrode materials currently used on neural interfaces display faradaic activity in addition to double layer discharging, and these materials include Pt and Ir noble metals, PEDOT, and iridium oxide.

1.3.1.1 Pt and Ir

The noble metals Pt and Ir have been widely used in neural interfaces, each individually as well as an alloy of the two [69], [71], [89], [90]. Current flow to tissue happens via capacitive and faradaic mechanisms, with the latter occurring through a surface oxide monolayer [42], [91]. Having the highest Young's modulus of all metallic elements, iridium is especially useful for fabrication of wire electrodes with sub-100 µm diameters that do not deform when inserted into tissue. These materials can be used in bulk form to create wire electrodes, or they can be deposited as thin films on electrode substrates using physical vapor deposition (PVD) techniques. As capacitance is proportional to surface area, use of PVD opens possibilities of creating roughened electrode films to increase electrode surface area and improve current transfer from electrode to tissue. Such efforts have included depositing Pt on a roughened substrate to

reduce impedance at the electrode interface [92], as well as the development of platinum black, a platinum film with a relatively rough surface morphology [93]. Pt and Ir are very corrosion resistant and have demonstrated ability to function *in vivo* for years [41], [71], but are generally less preferred compared to other materials with innately superior charge-transfer characteristics.

1.3.1.2 PEDOT

Poly(3,4 ethylenedioxythiophene) (PEDOT) is a conductive polymer that is used to improve the charge transfer characteristics of base electrode materials. PEDOT films are created from solution on pre-existing electrode sites through electrochemical techniques such as galvanostatic deposition. These films increase the surface area of the preexisting electrode as well as introduce faradaic mechanisms of charge transfer, and have been reported to reduce impedance by multiple orders of magnitude for platinum, iridium, and carbon fiber electrodes [62], [94], [95]. Being a polymer matrix, PEDOT can be seeded with additives that promote enhanced tissue interactions, such as the anti-inflammatory agent dexamethasone or the RGD adhesion peptide sequence [96], [97]. With a Young's modulus of ~2 GPa [98], PEDOT is softer than metallic electrode materials by two orders of magnitude and thus better matched to the stiffness of neural tissue, although still much stiffer than such tissue (~1 kPa). PEDOT has superior charge transfer characteristics to many materials and demonstrated functionality for at least 6 weeks *in vivo* [94], [95]. However, its reliability has not been proven for time periods of a year or more, its method of deposition can be prohibitive for microelectrode batch fabrication, and evidence exists that links the leeching of PEDOT deposition byproducts

to persistent tissue inflammation [96].

1.3.1.3 Iridium oxide

Similar to PEDOT, iridium oxide (IrO_x) is created as a thin film and is characterized by large surface area as well as faradaic charge transfer with ionic environments. This mechanism occurs via Ir transformation between the Ir^{3+} and Ir^{4+} oxidation states in oxidized iridium film, [42], [99], which can be formed via electrochemical cycling of iridium substrate, thermal decomposition, direct electrodeposition, or reactive sputtering [100]–[106]. Of these methods, reactive sputtering is often preferable due to its ease of tailoring for batch fabrication and cleanliness. In reactive sputtering, an Ar/O plasma impinges on a target of pure iridium, dislodging Ir atoms that become oxidized as they deposit on the electrode substrate. Characteristics of the IrO_x film such as its dendritic structure or internal stress can be controlled by adjusting gas flow and pressure [107], [108]. IrO_x films have lower impedances than noble metals by an order of magnitude or more [104], [108] and have demonstrated functionality *in vivo* for periods of months to over a year [74], [106]. For these reasons, IrO_x is a valuable electrode material for use on neural microelectrodes.

1.3.2 Conductor materials

Neural microelectrode conductors transfer current between exposed electrodes and hardware interconnect sites, and have few constraints on material choice aside from being sufficiently bio-inert and low resistance. Conductor material choice is primarily determined by the specific design and architectural choices made in constructing a

microelectrode device. Conductor materials in use include noble metals such as gold, platinum, and iridium, other metals such as tungsten and stainless steel, as well as carbon fiber and even highly doped silicon. While reports of damage or challenges regarding conductor materials are generally infrequent, the susceptibility of tungsten microwires to degradation *in vitro* and *in vivo* is widely known [70], [109], [110].

1.3.3 Dielectric materials

Dielectric materials must prevent contact between the ionic physiological environment and microelectrode conductors. They ensure the integrity of the electrode-interconnect path and prevent signal shunting to non-target regions of the tissue environment local to the implant, as well as the recording of biological noise stemming from recording the activity of non-target neurons [40], [111]. Thus, in contrast to electrode materials, dielectric encapsulation must ensure that impedance does not decrease over time, as such a reduction may indicate the development of shunt paths through encapsulation.

Microelectrode dielectric materials should have a low dielectric constant to reduce parasitic capacitance, strong adhesion to substrate, conductive, and electrode materials, and demonstrated resilience and nontoxicity to the *in vivo* environment. A low water-vapor transmission rate (WVTR) is also desirable, as it reduces the likelihood that fluid ingress into the material will affect the previously mentioned properties [112]. An additional requirement for microelectrodes is that the dielectric material be readily fabricated or deposited in a manner appropriate for micrometer-scaled devices. Common dielectrics in use for commercial neuromodulation and cochlear implant electrodes

include silicone and polyurethane derivatives [113], [114], which have dielectric constants of ~3-4 and WVTR of 1 g mm m^{-2} day^{-1} or more. However, manufacturing methods and limitations largely restrict the use of these materials on microelectrodes. Materials that have been commonly employed for neural microelectrode dielectric encapsulation include polyimide, silicon dielectrics (silicon oxide and nitride), and parylene [115].

1.3.3.1 Polyimide

Polyimides are flexible polymers commonly formed by reacting a diamine with a dianhydride. The fabrication method often requires wet chemistry such as spin or dip coating, and curing at high temperatures (~300 °C) [116]. These curing temperatures are accompanied by a high thermal tolerance for polyimide that makes their use particularly attractive for microfabrication processes that require high temperature exposure, such as some plasma and PVD methods. WVTR for polyimides has been reported in research and industry reports as ranging from 0.05 to 0.4 g mm m^{-2} day^{-1}, depending on measurement method, and dielectric constants have been given as a range from 2.9-3.5 [112], [115], [117]. These properties are comparable or superior to those of silicone or polyurethanes in commercial use, and polyimide has been widely employed on neural interface devices that are fabrication using planar substrates, as well as on dip-coated wires and shanks [70], [109], [118]–[120]. However, polyimide has been noted to suffer from adhesion failure as well as cracking and damage in both bench top *in vitro* as well as chronic *in vivo* tests [70], [109], [121]. In addition, the necessity of dip or spin coating do not render it ideally suited for creating conformal films on devices with high topography [122].

1.3.3.2 Silicon dielectrics

Silicon dioxide and nitrides are widely used in the semiconductor industry for integrated chip fabrication, and have been employed for neural electrodes [39], [76], [123]. Silicon oxide and nitride films that conform to high-topography devices can be created through chemical vapor deposition (CVD), resulting in films with strong adhesion. As ceramics the WVTR of these materials is orders of magnitude lower than those of polymers [124], and the dielectric constant of 3.9 for silicon dioxide is the standard criterion for low-κ dielectrics, while that of silicon nitride is higher at ~7. However, CVD silicon dioxide and nitride are known to be degraded *in vivo* [76], [125]. *In vitro* work has suggested film resilience may be improved using a multilayer oxide-nitride-oxide (ONO) architecture [121]; however, the increased processing required by such procedures render single-step material solutions more preferable.

1.3.3.3 Parylene C

Poly(p-xylylene) (parylene) is a polymer composed of aliphatically-linked benzene rings. Deposition of parylene films occurs through vaporization of parylene dimer above 100 °C, followed by pyrolysis of the dimer bonds around 670 °C and polymerization on the substrate at room temperature [116], [126]. This process result in conformal films nanometers to micrometers in thickness, and deposition imparts minimal thermal stress on the substrate or device. Several parylene variants exists, with parylene C (poly(chloro-p-xylylene)) being widely used on medical devices and neural interfaces [41], [65], [71], [115], [127]–[131]. Parylene C widely employed for its conformal deposition as well as its dielectric constant of ~3, and strong ion barrier properties with a

WVTR of 0.08 g mm m^{-2} day^{-1} [132]–[134]. It is a USP class VI polymer, a rating given to the most bio-inert materials and often cited to further justify parylene C use [2], [24], [63], [135]–[138], but which must always be accompanied by testing for appropriate tissue responses to parylene C within the context the medical device employed, pursuant to ISO 10993. The mentioned characteristics make parylene C strongly attractive for use as a dielectric for neural interfaces. However, undesirable impedance reduction, cracking, and erosion of parylene C has been observed for devices tested *in vitro* as well as chronically implanted microelectrodes, and linked to device failure [26], [69], [71], [73]–[75], [133]. The nonideal performance of parylene C underscores the need for better neural electrode materials and designs, and is a strong motivator for this work.

1.3.4 Penetrating microelectrode device types

Three common neural microelectrode device types exist that make use of the materials described thus far, and that are regularly employed in chronic *in vivo* studies. These are microwire arrays, planar silicon micromachined arrays (commonly known as Michigan electrodes), and three-dimensional silicon micromachined arrays (commonly known as Utah electrode arrays).

1.3.4.1 Microwires and microwire arrays

Microwires are arguably the simplest neural electrode architecture, being comprised of an insulated wire with a noninsulated tip and diameter around 100 µm or less. The small diameter is chosen to minimize tissue damage, and microwire electrodes have been shown to induce less tissue damage than other architectures [139]. Wire

materials with high modulus are required in order for the electrode to be inserted into tissue without becoming deformed. For wire diameters ranging from 25 to 125 µm, tungsten, platinum, iridium, and stainless steel microwires have been used [41], [70], [71], [90], [140], [141]. To further improve the biological response and reduce the FBR, recent development has focused on the use of carbon fiber electrodes with 7 µm diameter [62], [65], [131], [142]. While these devices can be inserted as single electrodes, use of microwire arrays is common to increase channel count and neural signal recording capabilities. Microwire conductor materials are the wires themselves, and electrode sites may be unaltered or they may be modified for improved electrochemical properties, such as through a PEDOT coating [62]. Dielectric encapsulation utilized has included polyimide and parylene C. Chronic recording of neural signals using microwires has been performed in animals, but no work in humans has been performed to date.

1.3.4.2 Michigan electrodes

In contrast to the relative simplicity of microwire arrays, Michigan electrodes take advantage of IC micromachining processes to create penetrating electrodes that can incorporate IC components. Pioneered by Wise *et al.* at Stanford University and further developed and commercialized at the University of Michigan, Michigan electrodes are fabricated on planar silicon substrates, which are patterned and etched to create sharp silicon shanks that can house electrodes and circuitry [80], [143]. Such a fabrication strategy is not limited to silicon, as conductive and insulating films can be patterned on any planar substrate that is compatible with microfabrication processing. Electrode patterns can vary widely, with the most common arrangement being along the length of

the penetrating shank. To avoid electrode crosstalk, the surface of the substrate/shank material must be insulating. Conductor materials such as gold and platinum are typically deposited using PVD and patterned intro individual channel traces through lithographic techniques. Dielectric encapsulation for these devices has been reported to include silicon oxide, silicon nitride, and parylene C [109], [123]. Different electrode materials have been investigated using Michigan electrodes, including IrO_x, PEDOT, and more experimental materials like carbon nanotubes [95], [144]. However, despite extensive development and flexibility in processing, Michigan-style electrodes have been noted to be unreliable for chronic recording applications in animals [139], [145], and have yet to be employed in humans.

1.3.4.3 Utah electrode arrays

Developed by Normann *et al.* at the University of Utah [146], the Utah electrode array (UEA) is a three-dimensional array of silicon tines with electrode sites exposed at the tips (Figure 1.1). Silicon micromachining occurs via a series of physical and chemical shaping techniques that have been developed over decades [122], [147], [148], which are capable of UEA batch-fabrication and customization of electrode pitch and length for different applications [35], [149]. The UEA is distinct among neural electrode technologies for its use of doped silicon (0.01-0.05 Ω cm resistivity) as both an architectural substrate, as well as the conducting material between electrodes and external hardware adapters. Electrode materials are deposited at silicon tips to improve charge transfer between the silicon array and tissue, with sputtering of Pt and IrO_x the commonly preferred method due to the compatibility of PVD processes with UEA fabrication.

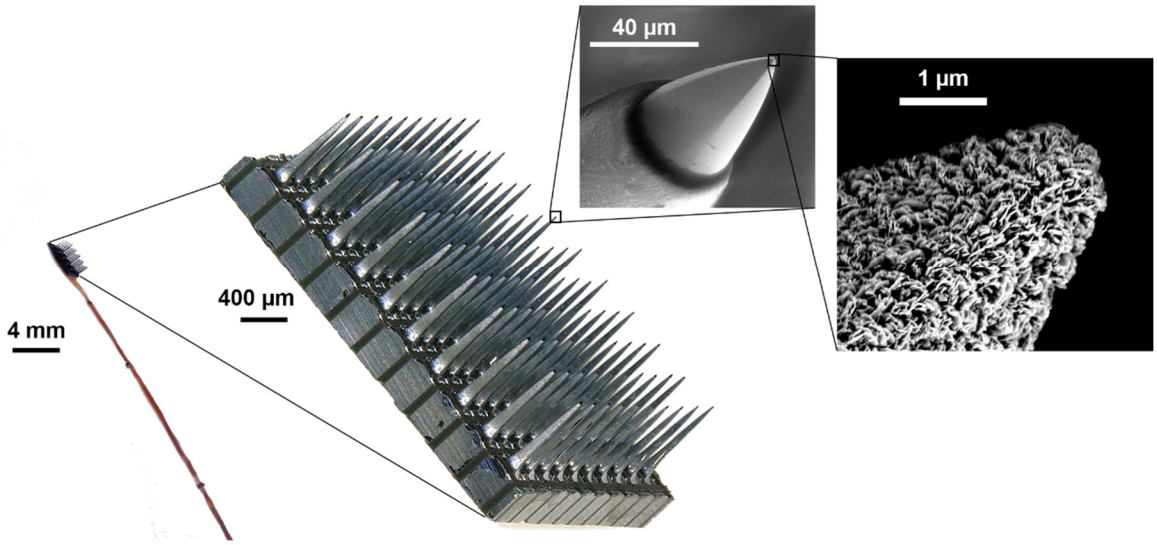

Figure 1.1 A UEA is shown at left assembled and bonded to a gold wire bundle, the interconnect between the array and external hardware. Magnification of the array shows the silicon-micromachined structure of individual silicon tines that penetrate neural tissue. A scanning electron micrograph shows magnification of the electrode region, with the electrode tip exposed through a parylene C coating. Final tip magnification shows the dendritic, high surface area structure of IrO_x that is deposited on UEA electrode tips.

Dielectric encapsulation of UEAs has included the use of polyimide and silicon nitride [72], [122], [147], but due to the previously mentioned advantages of parylene C, it is currently the dielectric material for standard devices. While biotic challenges to UEA use are known to exist [58], the UEA is a well-established technology that has been in use for two decades [150], including acute and chronic applications in rodents, large animals, and humans, in both peripheral and central nervous systems [33], [69], [147], [149], [151]. It is the only penetrating microelectrode device FDA-cleared for human use, and has been shown in multiple human trials to successfully enable control of neuroprosthetic devices [33], [36], [37], [152]. It has a form factor similar to microwire arrays, and undergoes a silicon-based manufacturing process similar to Michigan probes. Furthermore, material damage to implanted UEAs, particularly to parylene C film, has

been documented by several groups [26], [69], [74], [75], providing a strong dataset against which further research may be compared. For these reasons, this work employs the UEA as a representative neural microelectrode device for investigating strategies to improve microelectrode performance, which includes addressing issues not only with microelectrode array design, but also characterization and testing methods.

1.4 Microelectrode characterization and testing

The final test for any neural electrode is implantation and operation *in vivo*, with reliable recording and/or stimulation of neurons over time the metric of success. Metrics for such are commonly signal-to-noise ratio (SNR) of neural recordings, and stimulation thresholds, respectively. However, *in vivo* experiments are time-consuming and costly, and do not lend themselves to rapid evaluation of technological developments to drive informed design. Furthermore, detailed determination of failure modes *in vivo* is difficult if based on device functional performance alone. Additional characterization and bench top *in vitro* testing techniques are valuable tools to understand and predict electrode performance before investments are made for *in vivo* evaluation. The subsections that follow outline common methods in use and how they apply to this work.

1.4.1 Characterization methods

Sophisticated histology, imaging, and modeling techniques for characterizing the biotic response to neural electrodes have received attention and are the focus of ongoing work [51], [54], [58], [61], [153], [154]. However, beyond equipment improvements, little development or change to abiotic characterization techniques has occurred since

early reports of neural electrodes that paired electrochemical characterization with electron microscopy [41], [90], [143]. These methods, particularly electrochemical impedance spectroscopy (EIS) and scanning electron microscopy (SEM), are the predominant ways by which the state of neural microelectrodes is assessed.

1.4.1.1 Electrochemical characterization

Electrochemical techniques measure current-voltage relationships of an electrode within a solution. These measurements require an ionic solution, the electrode to be assessed (the *working* electrode), a *counter* electrode through which current can pass with little resistance (*e.g.* a large area Pt electrode), and a *reference* electrode that carries no current and maintains a constant voltage within the solution (*e.g.* an Ag|AgCl electrode). Measurements are aided by a potentiostat, which controls the voltage differential between the *working* and *counter* electrodes to drive a target voltage between *working* and *reference* electrodes. The current through the *working* electrode and the voltage between *working* and *reference* are measured for electrochemical characterization. In this way, confounding effects of an unknown voltage across the *counter* electrode due to electrochemical reactions or the activity of the electrical double layer are avoided, permitting confident measures of *working* electrode properties.

Three electrochemical techniques are commonly utilized to characterize neural microelectrodes, two of which are primarily used to assess performance of electrode site material. These are cyclic voltammetry (CV) and voltage transient (VT) methods. In CV, voltage is linearly swept between two limits at a constant rate, and current is measured. In VT measurements, biphasic current pulses are increased in amplitude until a voltage limit

is reached. The negative and positive voltage limits generally used for these techniques are -0.6 and +0.8 V with respect to Ag|AgCl. These are taken to be the points at which hydrogen and oxygen gas evolution occur, respectively, for a Pt *working* electrode, outside of which damage to tissue or electrode material is likely to occur [42], [86], [89], [155]. This range is referred to as the water window, and the amount of charge that can pass through an electrode before the water window is reached is a measurement of electrode material/design effectiveness. For CV, this is the area of the curve integrated below 0 A (cathodal charge storage capacity CSC), and for VT, this is the integral of one phase of the current pulse (charge injection capacity CIC), both normalized to the surface area that the electrode site occupies on the base substrate (geometric surface area). Being measures of charge with respect to an artificially applied voltage, CV and VT are most useful for characterizing electrodes in stimulation applications. A third technique employed is electrochemical impedance characterization, particularly at 1 kHz frequency, which is applicable to recording and stimulating electrodes and is universally employed for microelectrode characterization.

Impedance spectroscopy utilizes a small amplitude sinusoidal source signal of varying frequencies to measure amplitude and phase relationships between current and voltage, thereby providing an approximate spectral frequency response for an electrode. Low impedances for given electrode surface areas are targeted for electrode design, being associated with higher CSC, CIC, and SNR compared to higher impedance electrodes [62], [108], [123], [144]. It is not uncommon for only the impedance at 1 kHz to be monitored, being of chief interest due to the 1 msec characteristic period of a neural action potential [156]–[158]. The ideal electrode is considered to maintain stable

impedances over time, with increases in impedance possibly indicating damage to electrode site material, and decreases in impedance related to degradation of dielectric encapsulation. Repeated observation of the latter has motivated efforts to investigate encapsulating strategies that demonstrate improved impedance stability compared to materials in common use [133], [159]. However, the appropriateness of utilizing impedance data from only the 1 kHz frequency point to make broad deductions of neural electrode condition has been debated [109]. Wide-spectrum impedance is analyzed in the present work to better understand how impedance correlates with electrode condition, and evaluate the accuracy of utilizing only 1 kHz impedance to characterize electrode performance.

1.4.1.1 Physical characterization

Characterization of the physical state of a microelectrode complements electrochemical characterization, in that changes to impedance may be correlated to material changes/damage. Microscopy is used for this purpose, and the high resolution of SEM has proven especially valuable. Improvements to SEM systems over time have increased the quality and capability of SEM characterization, such as enabling the imaging of residual tissue adhering to explanted electrodes [75]. Back-scatter electron imaging (BSE), which assigns brightness proportional to atomic number, is especially valuable for characterizing UEAs due to the high brightness of IrO_x electrode metal compared to parylene C and silicon. SEM has been used to detect material damage and electrode failure modes incurred from chronic *in vivo* use, but it is ill-equipped to characterize changes to material chemistry that may provide clues to those failure modes.

Limited effort has been reported to characterize electrode materials using energy-dispersive X-ray spectroscopy (EDS) and Fourier-transform infrared spectroscopy (FTIR) [56], [110], and little information concerning material changes was obtained. However, reports utilizing SEM and FTIR to evaluate *in vivo* environmental stress cracking of polyurethanes uncovered chemical markers of failure, which were used to inform better material design as well as develop improved bench top tests of robustness [160]–[162]. Part of the present work evaluates more thorough use of such spectroscopic characterization methods for neural microelectrodes, so that SEM and EIS data may be complemented to similarly reveal *in vivo* failure modes and inform better designs and test methods.

1.4.2 Testing methods

Bench top testing of microelectrodes is an important step to determine electrode design effectiveness, before costly *in vivo* tests are undertaken. Tests of electrode mechanical rigidity for penetrating neural tissue have successfully informed designs and systems for implanting extremely small or flexible electrodes in cortex [64], [131], [163]. However, while tissue mechanical properties may be readily measured and simulated, the impact of chronic *in vivo* exposure on material integrity is not easily ascertained. The known salinity and temperature of the extracellular physiological environment has been referenced for artificial aging tests, which approximate *in vivo* conditions using phosphate buffered saline (PBS) at 37 °C [76], [135], [159], [164]. In order to obtain measures of material resilience within a reasonable timeframe, accelerated aging is

approximated by increasing the aging bath temperature, according to the empirical Arrhenius equation [165]

$$f = 2^{\frac{T-37°C}{10}} \quad . \tag{1.1}$$

In Equation 1.1, f is the acceleration factor, and T is the aging temperature. Thus, by increasing aging temperature to 67 °C, one year of exposure to physiological conditions can be approximated in 1.5 months. This is one method of simplifying actual implant conditions for the sake of efficient material and design testing. Another method is to forgo the use of functional electrodes themselves in favor of test structures, simplified devices that are less expensive to fabricate and that can evaluate electrode material performance in isolation, absent confounding factors inherent in microelectrode complexity. One such test structure in use is the interdigitated electrode (IDE), a planar device with metal traces patterned to form a capacitor with impedance highly sensitive to changes at its surface. IDEs have been utilized to evaluate the properties of dielectric encapsulation [135], [159], [164], [166], [167], including for neural electrode applications. However, discrepancies have been noted between results from normal IDEs and those with added topographic features, implying that IDE results may not hold for applications to fully fabrication neural electrodes with varied topographies [159]. Part of the present work addresses this testing discrepancy by comparing aging results from IDEs with varied topography against data from fully fabricated UEAs, to inform design of test structures that more accurately predict material performance on neural electrodes.

In addition to proper design of testing substrates, the test environment must also accurately reflect *in vivo* conditions. Accelerated aging in PBS based on Equation (1.1), while generally accepted within the neural microelectrode community, does not take into account the effects of the FBR. Constituents introduced through the FBR may make the environment more hostile to materials than a simple saline bath. For example, microelectrodes fabricated with a thermally grown silicon dioxide dielectric layer fared well during PBS aging tests, but failed during *in vivo* testing due in part to degradation of silicon dioxide and silicon [76]. As has been previously mentioned, damage to parylene C has been seen in several reports of *in vivo* exposure, but has not been reported for aging in PBS. Recently, an aging system for neural microdevices has been developed that reports to approximate 6 months' exposure to aggressive *in vivo* conditions in seven days [109]. This bath incorporates H_2O_2 in a PBS bath at 87 °C to simulate the effects of reactive oxygen species (ROS). This reactive accelerated aging (RAA) system is the first reported effort to advance the state of accelerated age testing of neural microelectrodes. A component of the present work evaluates the mechanism of RAA aging and its effectiveness of simulating *in vivo* material damage, utilizing spectroscopic characterization techniques in addition to EIS and SEM to identify damage markers.

1.5 Problem statement, approaches, and impact

The present work aims to advance strategies that will reduce the risk of dielectric encapsulation failure on neural microelectrodes, and utilizes the parylene C-encapsulated UEA as a reference device to advance state-of-the-art. Three independent yet interrelated approaches are employed, discussed at length in Chapters 2, 3, and 4, which address

material, testing, and characterization strategies to create improved frameworks for informed neural electrode design.

In Chapter 2, we investigate a novel hybrid encapsulation scheme composed of Al_2O_3 underneath parylene C, developed by our group and that has demonstrated superior impedance stability when compared to parylene C alone [136], [164]. However, characterization of this hybrid encapsulation has been largely limited to fully encapsulated planar test devices. Prior studies have exhibited very limited scope when evaluating performance within the context of nonplanar topography or functional neural arrays [133], [159]. Dielectric coatings over neural arrays must be resilient, in spite of features such as high aspect-ratio electrode shanks and dielectric barrier openings at the electrode sites. Our approach employs a battery of *in vitro* tests to determine how this hybrid coating performs when exposed to three different features common across microelectrode architectures. In addition, we evaluate its performance on properly functioning microelectrodes compared to devices lacking the Al_2O_3 base layer. To our knowledge, such a system of tests has never before been employed to evaluate any dielectric film, and this is the first study to evaluate Al_2O_3-parylene C encapsulated neural interfaces directly against interfaces encapsulated with parylene C alone. Chapter 2 results generate new knowledge concerning the value of this hybrid encapsulation, and show how the proposed *in vitro* testing paradigm can anticipate the performance or failure of any neural interface dielectric coating.

Chapter 3 investigates the prospect of mitigating shunt path risk through the use of conducting material that exhibits low volume resistivity, while at the same time showing high electrochemical impedance through physiological saline. A material with

these properties would readily permit signal conduction from an embedded electrode with little to no signal attenuation, while resisting shunt path formation, such as from dielectric coating damage. We are not aware of prior reports characterizing the use of any such material for this application. Our experience with UEA has suggested that degenerately-doped silicon is ideal for this purpose, a novel concept with significant implications on UEA design for impedance stability. Chapter 3 results address a gap in knowledge concerning the innovative use of materials in microelectrode architecture, to provide resilience against shunt path formation incurred through damaged dielectric encapsulation.

In Chapter 4, we advance the body of knowledge regarding parylene C damage incurred under *in vivo* conditions. Explanted parylene C-coated devices have been shown to exhibit film degradation and cracking [26], [69], [71], [110], and this has been directly linked to impedance reduction and neural signal loss [73]. However, analyses in these cases has been limited to electron micrographs and electrochemical characterization. More comprehensive chemical analysis can provide guidance towards the creation of both more resilient dielectric coatings, as well as *in vitro* test environments for more accurately predicting device performance. We possess a very unique dataset consisting of two UEAs explanted after >3 years in feline peripheral nerve, which exhibit similar parylene C damage mechanisms as those reported in [73], also after 3-year time point. Our analysis of these arrays using spectroscopic methods, including EDS and FTIR, provides the most in depth report of *in vivo* parylene damage to date, and we develop unique methods to permit interrogation of UEAs in such a manner. We correlate our findings to identical analyses performed on devices subjected to RAA protocols in order

to fill the gap in knowledge that separates bench top test methods and physiological conditions. Chapter 4 results advance the understanding of chemical burdens on implanted dielectrics and will further drive improvements to neural microelectrodes.

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CHAPTER 2

ANALYSIS OF AL_2O_3 – PARYLENE C BILAYER COATINGS AND IMPACT OF MICROELECTRODE TOPOGRAPHY ON LONG TERM STABILITY OF IMPLANTABLE NEURAL ARRAYS

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Analysis of Al_2O_3—parylene C bilayer coatings and impact of microelectrode topography on long term stability of implantable neural arrays

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Abstract

Objective. Performance of many dielectric coatings for neural electrodes degrades over time, contributing to loss of neural signals and evoked percepts. Studies using planar test substrates have found that a novel bilayer coating of atomic-layer deposited (ALD) Al_2O_3 and parylene C is a promising candidate for neural electrode applications, exhibiting superior stability to parylene C alone. However, initial results from bilayer encapsulation testing on non-planar devices have been less positive. Our aim was to evaluate ALD Al_2O_3-parylene C coatings using novel test paradigms, to rigorously evaluate dielectric coatings for neural electrode applications by incorporating neural electrode topography into test structure design. *Approach.* Five test devices incorporated three distinct topographical features common to neural electrodes, derived from the utah electrode array (UEA). Devices with bilayer (52 nm Al_2O_3 + 6 μm parylene C) were evaluated against parylene C controls ($N \geqslant 6$ per device type). Devices were aged in phosphate buffered saline at 67 °C for up to 311 d, and monitored through: (1) leakage current to evaluate encapsulation lifetimes (>1 nA during 5VDC bias indicated failure), and (2) wideband (1–10^5 Hz) impedance. *Main results*. Mean-times-to-failure (MTTFs) ranged from 12 to 506 d for bilayer-coated devices, versus 10 to >2310 d for controls. Statistical testing (log-rank test, $\alpha = 0.05$) of failure rates gave mixed results but favored the control condition. After failure, impedance loss for bilayer devices continued for months and manifested across the entire spectrum, whereas the effect was self-limiting after several days, and restricted to frequencies <100 Hz for controls. These results correlated well with observations of UEAs encapsulated with bilayer and control films. *Significance.* We observed encapsulation failure modes and behaviors comparable to neural electrode performance which were undetected in studies with planar test devices. We found the impact of parylene C defects to be exacerbated by ALD Al_2O_3, and conclude that inferior bilayer performance arises from degradation of ALD Al_2O_3 when directly exposed to saline. This is an important consideration, given that neural electrodes with bilayer coatings are expected to have ALD Al_2O_3 exposed at dielectric boundaries that delineate electrode sites. Process improvements and use of different inorganic coatings to decrease dissolution in physiological

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fluids may improve performance. Testing frameworks which take neural electrode complexities into account will be well suited to reliably evaluate such encapsulation schemes.

Keywords: neural electrodes, utah electrode array, accelerated aging, atomic layer deposited (ALD) Al_2O_3, parylene C, survival analysis, bilayer encapsulation

S Supplementary material for this article is available online

(Some figures may appear in colour only in the online journal)

1. Introduction

Sensorimotor prosthetics controlled by neural signals present exciting possibilities for amputees and locked-in individuals. Multiple degree of freedom control from cortical interfaces have already been demonstrated for an individual with tetraplegia [1–4]. Work is ongoing to create both recording and stimulating electrodes for closed-loop interfaces, so that through haptic feedback a sense of embodiment for the prosthetic limb can develop [5, 6]. However, clinical translation of penetrating neural electrode array technologies for chronic use is hampered by poor long term reliability of the implanted arrays. Recorded neural signals often fail months to a few years post-implantation [7–9], and the number of evoked percepts decreases with time.

For clinical viability, neural interfaces must be able to function *in vivo* for ten years [8] to at least have a lifetime similar to the battery life of typical implanted pulse generators (IPGs). Dielectric coatings provide a critical contribution to neural interface stability, by providing a barrier against crosstalk and shunting of electrical signals to non-target tissue regions. Materials used for this application include SiO_2 or SiN_x [10, 11], polyimide [12, 13], silicone [14], and parylene C [15–17]. In addition, recent reports detail the development and application of silicon carbide [18, 19] and chemical vapor deposited siloxanes [20]. However, an encapsulation scheme has yet to be recognized as capable of providing microelectrode performance stability for 10+ years [21]. Post-surgical reductions of electrode impedance have been repeatedly observed and attributed to dielectric degradation [2, 17, 22, 23], and encapsulation degradation is frequently cited as the mechanism for loss of recorded neural signals and reduced signal-to-noise ratio [11, 24–27]. To prevent such failure, new materials and methods are needed to advance the current state of dielectric encapsulation for implantable neural microelectrodes.

Recent reports have detailed initial investigations into the performance of atomic layer deposited aluminum oxide (ALD alumina), as a novel dielectric material for implantable electrodes and electronics [28–31]. ALD alumina has been shown to have a water vapor transmission rate (WVTR) as low as 10^{-10} g mm m^{-2} d^{-1} [32], compared to silicone for which manufacturers have reported a formulation-dependent WVTR range of 18–128 g mm m^{-2} d^{-1} [33, 34]. Materials with low WVTR are desirable for their stable dielectric properties, as they do not hydrate as readily as those with higher WVTR, and more effectively prevent water nucleation around device surface contaminants [35]. The exceptionally low WVTR of ALD alumina has made it attractive for organic light-emitting diode (OLED) applications, and films as thin as 50 nm have been shown to protect OLEDs against deterioration [36]. However, ALD alumina is known to degrade when directly exposed to water [37]. While tests of cell proliferation [38] and cytotoxicity (internal study) have found no detrimental effects from ALD alumina degradation products, protective capping layers are nevertheless required for the permeation barrier benefits of this film to be realized in humid environments, or during immersion [39]. The parylene family of polymers have been employed to this end: Kim *et al* reported the use of 1 μm parylene N as an ALD alumina capping layer for solar cell applications [40], and Xie *et al* evaluated 6 μm parylene C + ALD alumina as a dielectric coating for implantable devices [29, 30]. Parylene C is particularly attractive for implantable applications, for the outlined reasons which follow.

Parylene C is a USP class VI polymer commonly used as a medical device dielectric owing to its low dielectric constant ($\varepsilon_r = 3.15$), a WVTR smaller than other encapsulating polymers (0.08 g mm m^{-2} d^{-1} for parylene C compared to 0.4 for polyimide and 0.6 for parylene N) [33], and excellent chemical inertness. Importantly, both parylene C and ALD alumina are applied through vapor deposition processes which create highly conformal and uniform films, a significant consideration for the fabrication of microelectrodes with non-planar topography. While >4× improvement has been reported in accelerated aging lifetime for devices with the bilayer versus parylene C alone [29, 31], these tests were conducted on planar interdigitated electrodes (IDEs) lacking the topographical and material complexity that is commonly seen on multielectrode arrays (MEAs). Of results garnered from planar IDE tests, authors have acknowledged that the coating lifetime is difficult to extrapolate to functional microelectrodes [31]. Furthermore, preliminary work which introduced topography to IDEs found performance reduced by half for test samples so modified [29], and traced encapsulation failures to regions of abrupt topographical transitions [41]. Our report addresses the gap in knowledge concerning the long term performance of this bilayer when applied to complex and non-planar neural electrodes, and advances understanding of how the presence of topographical features and the ALD alumina film influence neural microelectrode stability.

For this work, we employ 4 × 4 utah electrode arrays (UEA) as a neural interface to test bilayer performance, preferred over standard 10 × 10 devices for improved study

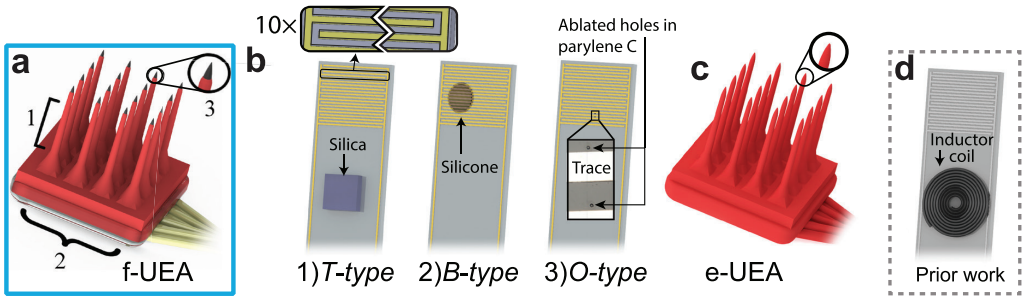

Figure 1. Illustrations of all 5 types of test devices used in this study are shown next to a model of an IDE with coil topography used in previous work [28] (IDEs and UEAs are shown at different scales). Where appropriate, encapsulation coatings are shown in red. (a) Topography of a functional UEA (f-UEA) consists of (1) electrode tines, (2) silicone backing, and (3) electrode openings. (b) IDEs designed to test the effects of features 1–3 model the effects of tines (*T-type*), backing (*B-type*), and openings (*O-type*). The encapsulation coating is not illustrated for clarity. (c) Completely encapsulated UEAs (e-UEAs) lack electrode openings, and incorporate both *T-type* and *B-type* features. (d) Devices used in prior work to study the effect of topography on encapsulation consisted solely of IDEs with offset inductor coils.

efficiency. From the UEA we derive topographical features present on diverse microelectrode architectures. The UEA is a well-established technology [1, 10, 42–44] that has 510(k) clearance from the FDA, facilitating Investigational Device Exemption clinical investigations. Ongoing human trials and data from non-human primate studies have underscored the need for improved UEA stability [10, 23, 45]. The topography which is encountered by the dielectric encapsulation of a functional UEA (f-UEA) has three principal parts, highlighted in figure 1(a). Feature type 1 consists of penetrating electrode tines extending out from the planar array base, which are commonly seen on 3D electrode arrays such as floating microwire arrays. Feature type 2 is silicone backing applied over an interconnect region where insulated gold wires are bonded to channels corresponding to each tine; dielectric failure in this region can contribute to crosstalk. A notable aspect of feature type 2 is that parylene C/bilayer encapsulation does not extend over silicone backing owing to significant fabrication constraints, instead the electrode tines and wire bond regions are encapsulated separately. Our test approach for feature type 2 evaluates the value of a continuous encapsulating film over silicone backing, to inform future microelectrode studies and designs. Feature type 3 is an opening in the encapsulation (deinsulation) to expose the electrode site, and is present on every penetrating electrode technology.

To evaluate interactions of bilayer encapsulation with individual features, IDEs similar to those previously reported are modified to approximate the three UEA topographies mentioned (figure 1(b)). These are subject to accelerated aging along with fully encapsulated UEAs (e-UEAs, figure 1(c)), which lack feature type 3 of electrode site openings. The high intrinsic impedance of IDEs and e-UEAs, which as a group will be referred to as *test structures*, enables sensitive resolution of dielectric degradation and shunt path formation using standard impedance spectroscopy methods. We compare the impedance stability over time of these devices with that of f-UEAs, as well as to prior work (figure 1(d)), and draw conclusions on how bilayer encapsulation influences neural electrode stability, and in turn is influenced by the topography.

2. Methods

Our experimental approach builds on prior encapsulation studies by adding complexities associated with the device topography, mechanical forces, and encapsulation defects relevant to neural arrays. By testing distinct features in isolation using IDEs, we can identify feature-associated failure modes that are difficult to isolate from baseline neural implants. IDE devices allow us to investigate the intrinsic properties of the encapsulation material, due to fewer effects from topography, mechanical forces, and defects (e.g. tip exposure). IDE results can be compared to those of e-UEAs, which are comprised of a more complex topographical feature set but which exhibit high intrinsic impedance similar to IDEs. Data from IDEs and e-UEAs can then be related to those of standard f-UEAs to understand the relative impact of encapsulation on UEA stability, and advance understanding towards robust dielectric films for neural electrodes.

2.1. Al_2O_3 and parylene C encapsulation

Preparation for encapsulation included test device sonication in acetone, followed by a rinse in methanol, isopropyl alcohol (all CMOS grade, JT Baker, Center Valley, PA), and deionized water, to remove surface oils. ALD alumina was deposited by plasma-assisted atomic layer deposition (PA-ALD) at 120 °C using a Fiji F200 (Cambridge NanoTech, Waltham, MA). Atomic layer deposition creates highly conformal coatings by building up thin films roughly one monolayer per cycle, and PA-ALD is reported to produce alumina films with higher density and fewer defects than thermal processes [46]. PA-ALD began with a 0.06 s vapor pulse of trimethyl aluminum (TMA) which was then purged with 10 s of argon flow. Oxygen plasma exposure (20 sccm O_2, 300 W at 13.56 MHz) for 20 s followed, with a 3 s final argon purge to complete one deposition cycle. Five hundred cycles were conducted at 0.3 mTorr base pressure to generate a film of 52 nm target thickness. Actual film thickness across device groups was reliably 50–53 nm, verified through ellipsometry (JA Woollam Co.,

Lincoln, NE) (400–1000 nm, 50° and 70°), using a Cauchy fit. Films deposited on polished silicon were found to have a cytotoxicity score of zero (indistinguishable from media and negative controls) according to MEM elusion assay protocols [47] (Nelson Laboratories, Salt Lake City, UT).

Vapor-phase A-174 silane adhesion promoter (Momentive Performance Materials, Waterford, NY) was used to enhance parylene C adhesion to test devices [48]. Devices were placed with a 3 ml open container of A-174 in a vacuum dessicator, which was left in an evacuated state for 2 h. Parylene deposition followed using to the Gorham process [48, 49], in a LabTop 3000 (Para Tech, Aliso Viejo, CA) or PDS 2010 (Specialty Coating Systems (SCS), Indianapolis, IN) (no difference in film performance or appearance was noted based on deposition equipment). Coatings were generated from DPX-C dimer (SCS), and film thickness was verified by surface profilometry (Tencor, Milpitas, CA) across a step-edge. Target parylene C thickness was 6 μm, with actual thickness consistently falling in the 6–7 μm range. All devices coated with ALD alumina + parylene C bilayer were statistically compared to parylene C-only controls, with parylene C films always deposited in the same run for a given set of experimental and control devices. Adhesion tests were performed per ASTM D3359, and acceptable parylene adhesion to ALD alumina-treated and control substrates was consistently found.

2.2. Fabrication of test devices

Five different device types were used to evaluate bilayer encapsulation using topographies and structures representative of neural electrode topography and mechanical characteristics, as illustrated in figures 1(a)–(c).

2.2.1. Interdigitated electrodes. As has been previously described [28, 31], IDEs were fabricated by patterning sputter-deposited Ti/Pt/Au (100/150/150 nm) on fused silica wafers (Hoya, Tokyo, JPN) using standard photolithography lift-off techniques. The IDE field consists of ten separated electrode pairs that are 5 mm long with 130 μm width and 260 μm pitch, connected to two solder pads. Patterned wafers were diced to singulate IDEs before further processing introduced desired topographical features. Features simulated the presence of high aspect ratio tines (*T-type*), silicone backing (*B-type*), or electrode openings (*O-type*), as described in figure 1(b) and detailed in sections 2.2.1.1–2.2.1.3. Prior to encapsulation, PTFE-insulated copper wires were soldered to pads to facilitate electrochemical measurements, and solder joints were potted with MED-4211 silicone (NuSil, Carpenteria, CA).

2.2.1.1. Tine-type IDE features. *Tine-type* or *T-type* test devices were fabricated by using M-31CL medical-grade epoxy (Loctite, Dusseldorf, DEU) to attach $3 \times 3\,mm^2$ squares of fused silica 1 mm in height to IDEs. Squares were placed on the test samples away from the IDE field, a positioning paradigm previously used when introducing inductor coil topography to IDEs [29] (figure 1(d)). This choice in topography and placement was selected for two reasons. First, the vertical sidewalls of the silica insert were deemed a suitable approximation to the near-vertical tines on the UEA. Second, while the placement of the silica insert away from the IDE field was expected to mute its effects on *T-type* IDE performance, it permitted comparison to prior literature. To maximize sensitivity to encapsulation breakdown, topographic features for remaining IDEs were placed over IDE fields.

2.2.1.2. Backside-type IDE features. *Backside* or *B-type* devices were created by curing approximately 0.1 ml of MED-4211 silicone over the IDE field, occupying a circular area of 2.5 mm diameter. As the potting of UEA wire bonds with silicone is typically done by hand, this process and the generated topography were chosen to due to its similarity to those of UEAs. However, silicone placement for *B-type* IDEs occurred *before* encapsulation, different from silicone potting of standard UEAs which occurs *after* encapsulation. Current UEA fabrication protocols do not result in the formation of a continuous encapsulation layer over the electrode tines as well as the backside silicone; rather, the penetrating tines are encapsulated only to the array sidewalls. Silicone is then potted over the wire bonds and made to overlap sidewall encapsulation. *B-type* IDEs were designed to evaluate the performance of a continuous encapsulating film over silicone backing, and inform future UEA development pertaining to the value of such a feature. Preliminary work with *B-type* IDEs has indicated that such topography interacts well with bilayer encapsulation, with results showing IDE stability for >60 d in PBS at 67 °C [41]. The comprehensive design of the current work employs larger sample sizes and experimental times for more robust statistical analysis, to add to published data and enhance understanding of the encapsulation paradigm in question.

2.2.1.3. Opening-type IDE features. *Opening type* or *O-type* IDEs were wired and encapsulated prior to incorporation of *O-type* features. After encapsulation, two 10 μm diameter holes were ablated in parylene with a KrF excimer laser (Optec, Frameries, BEL), with each hole ~30 μm away from the edge of an electrode trace. Ablated surfaces were verified through optical inspection and cleared of carbon residue by etching in an oxygen plasma for 2 min (March Instruments, Westlake, OH) [50]. A 2 min etch in buffered oxide etchant (BOE) (Transene, Danvers, MA) followed to ensure Al_2O_3 removal in the ablation zone; parylene-only encapsulated IDEs were subject to an identical treatment. This feature simulated the presence of encapsulation openings around an electrode site, and facilitated analysis of encapsulation integrity in regions surrounding what are, in essence, deliberate encapsulation defects.

2.2.2. Utah electrode array fabrication. UEA fabrication has been previously described at length [30, 42, 51, 52]. Briefly, boron-doped silicon (0.01–0.05 Ω cm, Virginia Semiconductor, Fredericksburg, VA) was diced, processed and etched to form arrays of sharp tines 1–1.5 mm in length electrically isolated by glass-filled kerfs. The tips of the tines were sputter-coated with iridium oxide tip metal [53], and platinum was deposited for wire bonding on the array backside. Final processing steps for e-UEAs and f-UEAs followed distinct courses and are described below.

2.2.2.1. Encapsulated UEAs. Fully encapsulated UEAs exhibit high impedance similar to that of IDEs, and therefore impart high sensitivity to impedance decreases resulting from relatively small areas of encapsulation degradation and shunt path formation. The topography of e-UEAs consists primarily of electrode tines and silicone backing, and therefore e-UEA results can be correlated with those of *T-* and *B-type* IDEs for a more complete understanding of topographical effects on encapsulation. To construct e-UEAs, polyester enamel-insulated gold (99% Au:1% Pd) bonding wire (Sandvik, Stockholm, SWE) was used to connect UEAs to custom gold-flashed connector printed circuit boards (PCBs) (Circuit Graphics, Salt Lake City, UT) using a manual wire bonder (West Bond, Anaheim, CA). Bond pads, wire and joints were then coated with MED-4211 silicone and cured prior to the final step of encapsulation, which proceeded according to section 2.1. PCB contact pads for connecting to external equipment were masked with Kapton® tape (3M, Maplewood, MN) during encapsulation deposition.

2.2.2.2. Functional UEAs. To fabricate f-UEAs, metallized arrays were placed on Kapton® tape to mask wire bond pads, and then encapsulated with parylene C. Following encapsulation, devices were removed from the tape using a razor and electrodes were prepared for parylene deinsulation by pressing electrode tips through aluminum foil to a depth of 50–100 μm. Devices were wrapped in foil such that only the punched tips were exposed, and parylene on the tips was etched in continuous oxygen plasma for 18–24 min. Visual observation of parylene C etching progress on a planar monitor sample informed plasma exposure. ALD alumina was removed from the tips of bilayer f-UEAs by etching in buffered oxide etchant (BOE) for 6 min; f-UEA controls were subject to identical treatment. Device processing was completed with wire bonding and silicone potting, as described for e-UEAs (note that wire bonding and silicone potting of f-UEAs occurred *after* ALD alumina and parylene C deposition).

2.3. Sample size and measurement criteria

Sample populations and study endpoints are provided in the results section. Sample sizes were chosen to be consistent with prior work [25, 29, 31] and maximized given timeline, fabrication, and yield constraints. Individual electrodes from UEAs were treated as individual samples for statistical analysis. Survival endpoint criteria were derived from data published by Minnikanti *et al* [31], and set at a minimum of 63% failure or at least 132 d soaking, with the former being preferred if possible. Being omitted from the survival study, f-UEA studies were taken to at least 100 d, and arrays were not terminated unless impedance reduction for all electrodes had not been observed for more than one month immediately preceding termination. Measurement intervals were determined on a device-specific basis, according to expectations of film performance based on published work, type of topography, and our prior experience.

2.4. Accelerated aging

Devices underwent *in vitro* aging in 6 ml vials (Wheaton, Millville, NJ); caps were modified to permit feed-through of wires for IDEs and UEAs. The feed-throughs were sealed with silicone, and UEA PCBs were fixed to caps with epoxy. Vials were filled with 0.1 M phosphate buffered saline (PBS) created by dissolving prepared tablets in deionized water according to manufacturer's instructions (Sigma Aldrich, St. Louis, MO) and placed in an incubation oven set at 67 °C (Sigma Systems, Mansfield, MA). The temperature was chosen according to accepted Arrhenius modeling of reaction acceleration to simulate physiological aging at an 8× acceleration factor f, according to (1) [54]; T_{test} is the testing temperature, 67 °C in our case.

$$f = 2^{\frac{T_{\text{test}} - 37\,^{\circ}\text{C}}{10}} \tag{1}$$

It has been noted that temperatures above 60 °C may introduce parylene degradation mechanisms not present in physiological conditions [31]. However, from both published [29] and unpublished work comparing device failures across temperatures, we have not observed evidence to suggest failure modes incurred at 67 °C deviate from those at physiological temperature.

2.5. Electrochemical characterization

Techniques for evaluating encapsulation include chronoamperometry of encapsulated *test structures* to measure leakage current under continuous bias, and electrochemical impedance spectroscopy (EIS) to investigate the frequency-dependent encapsulation characteristics. Defects in the encapsulating film typically manifest as an impedance decrease most pronounced at $<$1 kHz [25, 29, 31], and concomitant rise in leakage current to $>$1 nA. Leakage current measurements are valuable for sensitive detection of shunt path formation in high-impedance devices, e.g. *test structures*. The measurement protocol for *test structures* consisted of consecutive EIS and leakage current measurements for a given time point. Leakage current was calculated by performing 5 V chronoamperometry for 20 s, and averaging the values across the final 10 s duration. Transients associated with hardware sampling limitations and high impedance capacitive *test structures* occurred during the first 10 s, so the steady state current after 10 s was chosen. A binary failure criterion of leakage current $>$1 nA was used for survival analyses to evaluate *test structure* lifetimes, derived from standards for implantable electronics and prior work [29, 31]. Importantly, EIS measurements of *test structures* generally were taken until the group study endpoint regardless of device failure, to enable analysis of dielectric failure progression.

Leakage current measurements were not suitable for f-UEAs, which are fabricated with exposed electrode tips and would innately give leakage currents well over 1 nA. Thus, f-UEAs were excluded from leakage current measurements and associated survival statistics, and instead characterized via EIS alone. EIS was measured in a Faraday cage with a 25 mV

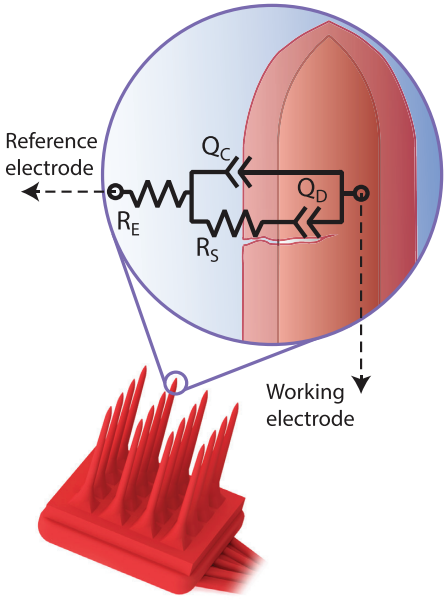

Figure 2. General circuit model used for fitting devices subject to circuit analysis. An example is shown of an e-UEA electrode with an encapsulation defect. R_E is electrolyte resistance, Q_C represents the semi-capacitive behavior of the electrode coating, R_S is a shunting resistance that bypasses the semi-capacitive layer (by way of charge transfer or encapsulation defect), and Q_D accounts for semi-capacitive characteristics at encapsulation defects, if present.

RMS source signal between 1 and 10^5 Hz at 10 points/decade. All measurements were done with a Reference 600 potentiostat (Gamry Instruments, Warminster, PA) and employed a two electrode configuration, performed between electrodes for IDEs, and between individual electrodes and a $>24\,mm^2$ area platinum wire electrode for UEA channels.

2.6. Survival and impedance analysis

Using the probability plot method [55], the Weibull distribution was identified out of common failure mode analysis functions (Weibull, lognormal, normal, exponential) as best fitting *test structure* survival data (figure S1 (stacks.iop.org/JNE/14/046011/mmedia)). The two-parameter Weibull probability density function was used as the fitting model:

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}}, \quad (2)$$

where β is the shape parameter, η the scale parameter, and $f(t)$ describes the prevalence of failure at time t. Devices that still met survival criteria upon study termination were right-censored at the last measurement time point for Weibull fitting. Mean-times-to-failure (MTTF) were calculated according to equation (3), where Γ represents the gamma function.

$$\mathrm{MTTF} = \eta\Gamma\left(1 + \frac{1}{\beta}\right). \quad (3)$$

The log-rank test, chosen for its applicability to censored survival data [56], was performed on survival distributions for each device cohort, to assess significant difference ($\alpha = 0.05$) between barrier coating failure rates.

EIS data were treated as being lognormally distributed, a decision based on our experience that lognormal processing techniques best represent EIS data behavior. Accordingly, we most commonly employed geometric averages and standard deviations, or averages and standard deviations of the base 10 logarithm of the data, for data visualization and statistical tests. Two-sample t tests performed on 1 kHz impedance data for bilayer versus parylene-only coated devices were conducted on the logarithm of the data, but corresponding data are shown on a log-scale plot for clarity. MATLAB with Statistics Toolbox (Mathworks, Natick, MA) and custom built log-rank function [57] was used for all statistical analyses.

2.7. Equivalent circuit modeling

To model electrochemical impedance characteristics, we employed constant phase elements (CPEs) to represent imperfect capacitance at interfaces between electrolyte and electrode coatings or dielectric defects. The CPE is commonly used to model combined capacitive and faradaic interactions within an ionic medium [58]. CPE impedance is defined by

$$Z_{\mathrm{CPE}} = \frac{1}{Q} \times (je)^{-n}, \quad (4)$$

where Q is CPE admittance and n is a constant between 0 and 1, describing behaviors between ohmic resistance and capacitance, respectively. The generalized circuit model we employed is shown in figure 2, adapted from [29, 59, 60]. R_E is resistance through electrolyte solution (PBS), and Q_C is the 'coating' CPE of the electrode under investigation. For *test structures*, this coating is the intact dielectric barrier; for f-UEAs it is the IrOx film exposed through deinsulation. R_S is a shunting resistance that bypasses coating capacitance, and can be attributed to the resistance through the dielectric layer for *test structures*. For f-UEAs with exposed IrOx, R_S is a combination of dielectric resistance and Faradaic charge transfer impedance at the metal surface, as EIS measurements were unable to distinguish the two. Instances of impedance loss over time correlated with a reduction in R_S, which represented the path of least resistance through dielectric encapsulation, e.g. emerging defects [60]. In these cases a 'defect' CPE (Q_D) in series with R_S was used to account for pseudocapacitive interactions at electrode regions exposed through defect evolution. Our model differed from prior studies, which have modeled electrochemical interactions at encapsulation defects by means of a double layer capacitance in parallel with a series combination of a charge transfer resistance and Warburg linear diffusion impedance [31, 61]. We implemented Q_D to accommodate the behavior of such a circuit while reducing the number of circuit parameters and risk of overfitting, to permit tracking of R_S over time. In general, all fitting was performed using the simplest circuit configurations possible. Parameters were deemed soundly modeled

Table 1. Summary of sample sizes, study endpoints, and number of failures (if applicable) for all devices.

Device type	Coating type[a]	Sample size[b]	Study endpoint[c] (d)	Failures (>1 nA leakage current)
T-type IDE	A + P	$N = 10$	331	6
	P	$N = 11$		10
B-type IDE	A + P	$N = 6$	211	3
	P	$N = 6$		1
O-type IDE	A + P	$N = 6$	11	4
	P	$N = 6$		4
e-UEA	A + P	$N = 48$ (from 3 UEAs)	311	26
	P	$N = 48$ (from 3 UEAs)		10
f-UEA	A + P	$N = 26$ (from 2 UEAs)	174	NA
	P	$N = 15$ (from 1 UEA)		NA

[a] A + P—bilayer coated devices. P—parylene-only control devices.
[b] IDE samples are individual devices, UEA samples are individual unbroken electrodes. All UEAs are 4 × 4 configuration.
[c] A + P and P devices for a given device type shared study endpoints.

if they were accompanied by error less than 5% parameter value, and all models had a goodness of fit <0.05. All modeling was performed with Gamry Echem Analyst, using the Simplex algorithm.

2.8. Failure analysis

We used copper electrodeposition to highlight any local regions of encapsulation breakdown and understand failure mechanisms for non-surviving devices. This technique worked on *test structures* with leakage currents >1 μA, which we observed was required for observable failure decoration. A constant voltage bias of up to 5 V permitted deposition, applied in copper acetate solution between a copper electrode and the failed *test structure*. Deposition was terminated once current exceeded 600 nA. Decorated devices were imaged with backscattered electron microscopy (BSEM) (FEI, Hillsboro, OR), utilizing the strong Z contrast of the metal relative to surrounding parylene C and silicon to identify copper decorations. The images were false colored with Photoshop (Adobe, San Jose, CA) to improve clarity. This method has been applied for IDEs in prior work to identify defects [41], but in the course of our study we found failed IDEs with high leakage current which could not be decorated with this method (deposition current <100 nA). This was due to the leakage path occurring predominantly underneath the encapsulation, rather than through it to the external environment, as will be further explained in Results. In these cases, target IDE regions were 'deactivated' through KrF laser ablation of IDE traces, and conclusions were drawn regarding the location of leakage current paths based on post-ablation electrochemical measurements.

3. Results

3.1. Overview

The data collected was used to measure the long-term stability and robustness of ALD alumina-parylene C bilayer encapsulation compared to parylene C controls for neural arrays and neural array features, with improved statistical power compared to prior studies. Table 1 summarizes our experimental design and survival results for IDEs and e-UEAs. The electrochemical performance from a combined total of 182 device samples was tracked for durations ranging from 11 to 331 d. Of devices used for survival analysis, 39 with bilayer encapsulation failed (56%) compared to 25 devices with parylene C alone (35%). Detailed analysis of survival dynamics and EIS characterization are given in the sections that follow.

Table 2. Summary of mean-times-to-failure (MTTF) for IDEs and e-UEAs.

Device type	Coating type	MTTF (d at 67 °C)	95% confidence interval
T-type IDE	A + P	450	100, 5800
	P	110	67, 200
B-type IDE	A + P	900	39, 1.7×10^6
	P	9.3×10^5	[a]
O-type IDE	A + P	12	1.2, 1200
	P	9.8	3.2, 74
e-UEA	A + P	510	260, 1200
	P	2300	390, 2.7×10^4

[a] Given the single failure point of *O-type* IDEs (P coating), 95% CI is very large.

3.2. Survival analysis

The MTTF of all *test structures* are given in table 2. *T-type* IDEs demonstrated considerable performance improvement (>4×) of the bilayer coating over controls. *B-type* IDE and e-UEA results showed the opposite effect, with bilayer coatings performing 4.5× worse than parylene controls for e-UEAs. The single failure for control *B-type* IDEs over the study duration of 211 d render the calculated MTTF of 1.1×10^8 d to be unreliable, but the data nevertheless indicates a longer survival time compared to bilayer coated *B-type* IDEs. *O-type* IDEs show MTTFs at least 10× smaller than those of all other devices, indicating rapid failure mechanisms not present in other device types.

Survival data is plotted in figure 3 as cumulative failure over time, and also includes Weibull fits and their associated parameters, which were used to calculate MTTFs in

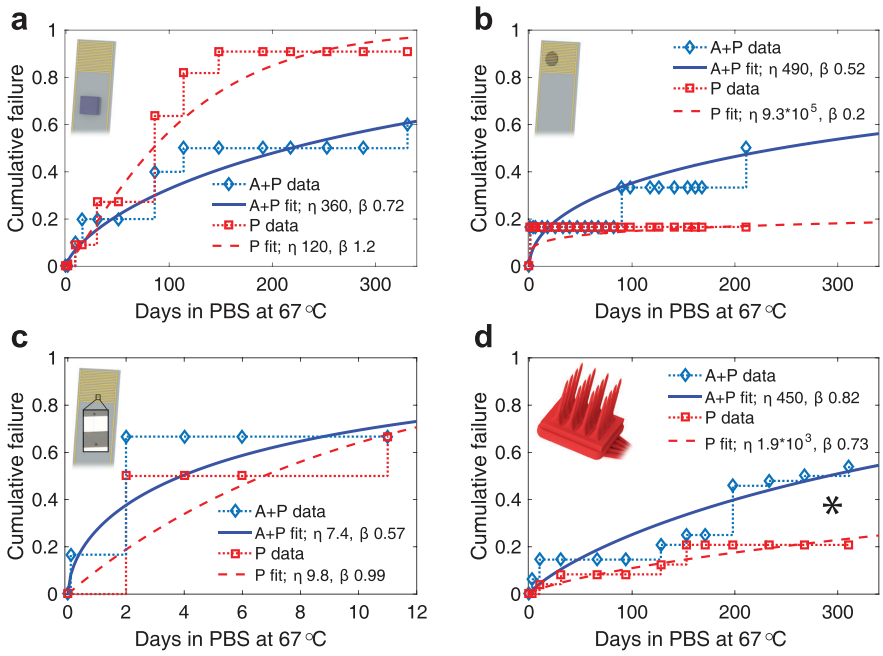

Figure 3. Survival plots showing data and corresponding fits to Weibull cumulative distribution functions, for devices with ALD alumina-parylene C bilayer (A + P) and parylene-only controls (P). Markers show measurement times. (a) T-type IDEs, (b) *B-type* IDEs, (c) *O-type* IDEs, and (d) e-UEAs (* significance difference between distributions according to log-rank test, $\alpha = 0.05$). Note that the time scale for (c) is distinct from the remainder, necessitated by short *O-type* MTTF. An illustration of each device type is shown in each plot for reference; Weibull fit parameters are given in the legends.

table 2. Survival curves for bilayer-coated devices have similar appearances, reflected in the shape parameter β which maintains values between 0.52 and 0.82 for all device types (note the different axis and η scale parameters for *O-type* devices). In contrast, control survival curves vary widely, with β spanning values between 0.2 for *B-type* devices to 1.2 for *T-type* devices. The Weibull shape parameter gives an indication of failure dynamics, with values <1 associated with systems dominated by early failure or infant mortality, and values >1 associated with a failure rate that increases with time. According to fitted β parameters, bilayer encapsulation consistently exhibited indications of infant mortality, while the control samples correlated with a much higher degree of variability or randomness in failure.

Log-rank tests of IDE survival data did not find statistically significant differences ($\alpha = 0.05$) between bilayer and control failure rates, with calculated p-values of 0.22, 0.57, and 0.91 for *T-*, *B-*, or *O-type* devices, respectively. While previous studies have noted improved performance of bilayer-coated planar IDEs compared to parylene C controls [29, 31], this study determined that these improvements do not translate to full electrode arrays, as determined by the log-rank test to statistically evaluate failure rates. Our results indicate that the effect size of bilayer encapsulation on device survival is smaller than previously suggested. Furthermore, it is apparent that the effect on lifetime is even negative compared to controls, when device complexity increases beyond planar *test structures*. This is emphasized by e-UEA data, for which log-rank testing did find statistically significant difference between coating failure rates ($p = 0.064$). Both larger sample size and increased device complexity may have played a role in effect detection for e-UEAs.

3.3. Test structure impedance

Wide-spectrum (1–10^5 Hz) impedance data for *test structures* were taken at every instance of leakage current measurement. Final data is shown in figures 4(a)–(d), segregated by device type. All impedances are shown as geometric averages, with colored regions corresponding to geometric standard deviation as described in the methods section 2.6. Impedances of surviving devices were similar regardless of encapsulation, thus for analysis purposes intact bilayer and control devices are treated as a single group, for each device type. Failed devices were discriminated by encapsulation type to understand how different coatings contribute to failure progression and associated impedance changes.

Non-failed *test structures* exhibited capacitive circuit behavior including a phase angle close to $-90°$ (not shown), and the concomitant decrease in impedance magnitude with increasing frequency. Impedance of intact IDEs ranged from 1 to 5 GΩ at 1 Hz, and decreased to 40–70 kΩ at 10^5 Hz, with *O-type* devices occupying the lowest end of each range. The average impedance of intact e-UEAs was higher than that of IDEs, decreasing from 18 GΩ to 270 kΩ across the measured spectrum. This higher impedance indicates a lower intrinsic

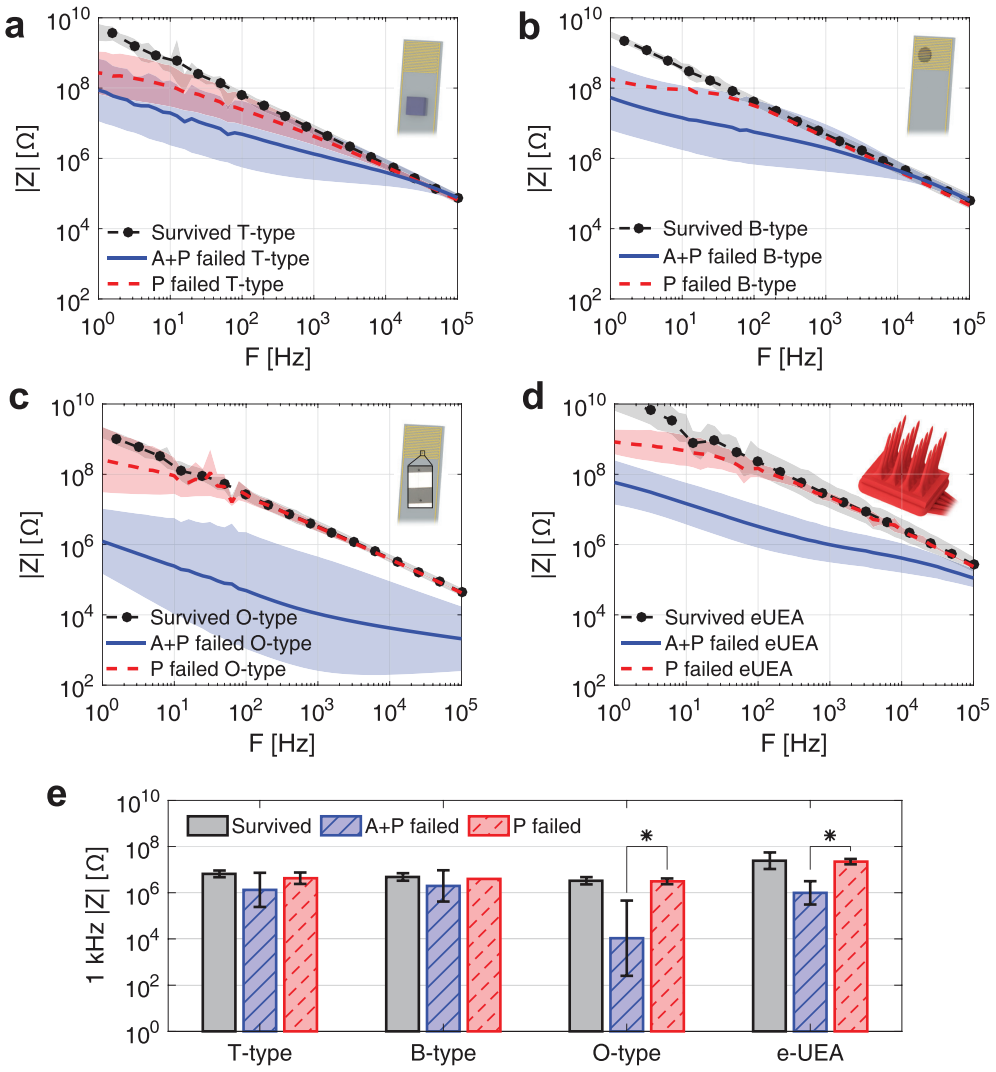

Figure 4. Geometric average endpoint impedance and accompanying standard deviation for all *test structures*: (a) *T-type* IDEs, (b) *B-type* IDEs, (c) *O-type* IDEs, and (d) e-UEAs. Insets are device illustrations for reference. Data for each device type is discriminated according to survival status at study end. Devices which survived are averaged together regardless of encapsulation type, while failed devices are segregated based on bilayer (A + P failed) or control (P failed) coating schemes. (e) Combined bar plot of 1 kHz impedances, asterisk denotes significant difference ($p = 0.05$).

capacitance of e-UEA electrodes compared to IDEs, owing to the 10× smaller surface area of the former (~0.4 versus 3.6 mm^2). Overall behavior of surviving devices was very consistent across all groups, with standard deviations no larger than three.

Failed *test structures* exhibited distinct and consistent trends based on the encapsulation scheme. The difference between failed controls and corresponding non-failed datasets was typically largest at 1 Hz, where average impedance of the former was ~0.2 GΩ for IDEs and 1.4 GΩ for e-UEAs, approximately 10× lower than surviving devices. At frequencies >100 Hz, impedance spectra of surviving and failed control *test structures* were indistinguishable for all but *T-type* devices. Nevertheless, *T-type* devices also approached non-failed behavior with increasing frequency. The group variance of failed control datasets also decreased with frequency, particularly illustrated by *O-type* IDEs which exhibit standard deviations decreasing from 8.5 to 1.0 over the spectrum.

The average impedance magnitude of failed bilayer coated devices universally exhibited greater change from intact devices than failed controls, with impedance reductions of up to 10^3× compared to 10× for controls. Average impedance at 1 Hz for non-surviving *O-type* IDEs measured 1 MΩ, while values for remaining *test structure* types ranged from 50 to 100 MΩ. Unlike failed parylene devices, decreased impedances persisted for all devices up to frequencies >10 kHz, at which

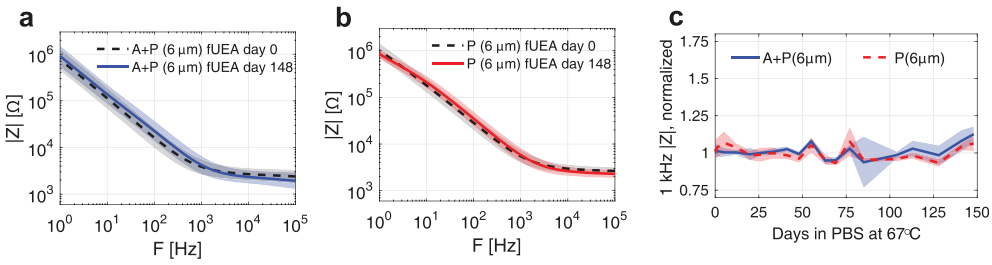

Figure 5. Impedance magnitude of f-UEA devices. Geometric average initial and endpoint impedances are shown with accompanying standard deviations for (a) bilayer (A + P) and (b) control (P) f-UEAs. (c) Time course of 1 kHz impedance change, showing *arithmetic* averages and standard deviations of all normalized channel data.

point failed *T-type* and *B-type* bilayer IDEs became similar to surviving devices. Impedances for failed bilayer *O-type* IDEs and e-UEAs fell below those of both surviving devices, as well as failed controls, across all frequencies. Variation within failed bilayer impedances was larger than that of surviving *test structures* or failed controls, with *O-type* devices demonstrating highest variance (standard deviation of 53) as well as lowest average impedance magnitudes (<10 kΩ).

A common metric of neural electrode performance is the impedance magnitude at 1 kHz, so chosen due to the association of this frequency with neural action potentials [59, 62–64]. Therefore, we conducted statistical analysis of 1 kHz impedance for surviving, failed bilayer, and failed control *test structures* (figure 4(e)). Average impedances for failed bilayer devices displayed the lowest values, being 1.3, 2.0, 0.01 and 1.0 MΩ for *T*-, *B*-, *O-type* IDEs and e-UEAs, respectively. Impedance magnitude of failed controls and surviving *test structures* were very similar for each device type, being 3–7 MΩ for IDEs and near 20 MΩ for e-UEAs. Two sample t-tests found significant difference ($p = 0.05$) between failed bilayer and failed control 1 kHz impedances for *O-type* IDEs and e-UEAs. The similarity of 1 kHz impedances for surviving devices and failed controls can be attributed to high impedance shunt path formation in the latter (shunt path impedance $>10\times$ that of 1 kHz impedance). While sufficient to cause failure according to the leakage current metric, such high impedance defects did not affect performance at 1 kHz, in contrast to the lower impedance shunting present for failed bilayer *test structures*. This is further analyzed and explained using circuit analysis, presented in a later section.

3.4. Functional UEA impedance

Figure 5 shows f-UEA soak testing results, with geometric average initial and endpoint impedance spectra plotted for each encapsulation scheme in figures 5(a)–(b). Typical impedance magnitudes of initial f-UEA measurements were close to 0.8 MΩ at 1 Hz, being largely determined by electrode tip exposure. Impedance decreased with increasing frequency in agreement with the pseudocapacitive phase angle of approximately $-70°$, consistent with previous IrOx electrode studies [53, 65], until an inflection near 1 kHz. At this frequency, the solution spreading resistance of ~1 kΩ was encountered and phase increased to $>-10°$, indicative of resistive behavior. While f-UEAs did not generally exhibit sustained impedance loss over time, a small indication of impedance decrease in f-UEA controls can be seen at frequencies <10 Hz. The implications of these impedance changes are further explored through circuit modeling in a later section.

The time course of 1 kHz impedance change for f-UEAs with and without ALD alumina is shown in figure 5(c). To accurately depict group performance despite variability imposed by tip exposure, 1 kHz impedance data points were normalized to the arithmetic average impedance over time on an electrode-by-electrode basis. The plots display the arithmetic average and standard deviation of the normalized impedance for all electrodes per encapsulation type. Normalized impedance oscillated between 0.9 and 1.1 during 148 d of monitoring, and increased after day 148 due to handling error during characterization which caused IrOx metal damage; for this reason average data is only shown for 148 d. In agreement with *test structure* data, f-UEA measurements do not indicate that bilayer films impart enhanced impedance stability compared to control films.

3.5. Principal component analysis of impedance

Principal component analysis (PCA) was employed to condense full spectrum impedance magnitudes for all devices into components of maximum variance, and permit visualization of *test structure* and f-UEA data in a single plot. The PCA dataset incorporated all endpoint *test structure* impedance spectra (see figures 4(a)–(d)), as well as initial f-UEA spectra (shown in figures 5(a)–(b)). Figure 6 shows the first two principal components, accounting for 98.8% of all variance within the full dataset. *Test structures* are segrated according to survival status as previously described. Initial f-UEA impedance spectra were chosen as a basis for best achievable neural electrode characteristics, defined by a single external current path through a low-impedance electrode. Surviving *test structure* data represent ideally functioning dielectric films, which prevent undesired current passage and shunting. These two groups have the tightest clustering and largest inter-group spectral variance, conveyed by the distance between centroids (large hollow symbols emphasized in inset). Their inter-centroid distance (ICD) of 12.1 represents the capacity for an intact dielectric coating to prevent the ocurrence of shunt paths which may infringe on microelectrode performance.

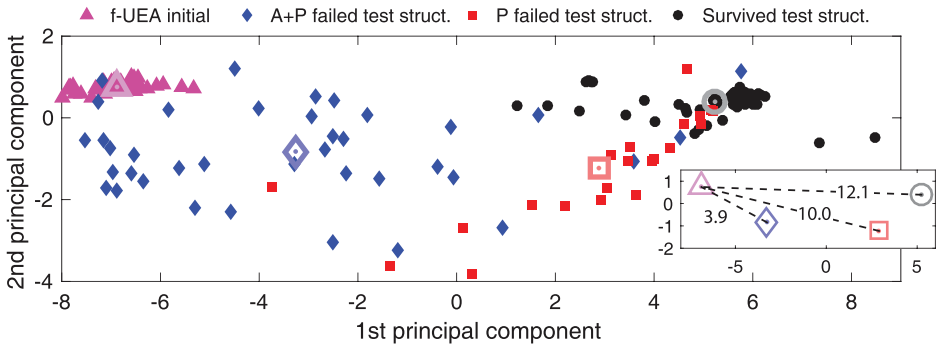

Figure 6. Principle component analysis of all *test structure* endpoint impedance spectra, against initial f-UEA spectra. *Test structure* data is differentiated according to survival status (see figure 4). Large hollow symbols indicate group centroids. Inset shows centroids alone with inter-centroid distances between f-UEA and remaining groups.

Failed *test structure* controls generally clustered near surviving devices and had an ICD of 10.0 with f-UEAs. In contrast, failed bilayer devices had a dispersed distribution, little overlap with intact *test structures*, and an ICD of 3.9. Smaller ICDs between f-UEAs and failed *test structure* groups indicate increased likelihood of encapsulation damage that may compromise electrode function, compared to surviving *test structures*. Failed parylene controls showed a 20% reduction in ICD with respect to surviving *test structures*, compared to 70% reduction for failed bilayer devices. This suggests that defects in parylene C encapsulation are less likely to impact neural electrode function than defects in bilayer encapsulation.

3.6. Circuit modeling

We utilized circuit modeling to analyze and interpret the time course of impedance changes during accelerated aging. In particular, modeling genrally provided a consistent means of characterizing encapsulation-dependent trends in impedance decreases over time, across different device types and performance characteristics. Figure 7 shows representative fitting characteristics and parameters for B-type IDEs and f-UEA electrodes, demonstrating how circuit model complexity increased in response to changing impedance spectra. Models were simplest for dry IDEs (figure 7(a)), which incorporated a dielectric coating CPE (QC, refer to figure 2) with nC = 1, equivalent to a simple capacitor (CC). A large shunt resistor in parallel (RS > 90 GΩ) completed the circuit. Submersion in PBS caused hydration of the polymer encapsulation, potential water ingress, and contribution of mobile ion activity to electrode behavior. This resulted in a transition from purely capacitive to constant-phase behavior for which the QC exponent varied 0.9 < nC < 1, as seen for an intact B-type device after 211 d (figure 7(b)). To model the failed bilayer B-type IDE shown in figure 7(c), two key changes were made with respect to the intact IDE equivalent circuit: (1) a drastic reduction in R_S (>4 orders of magnitude), and (2) the incorporation of the defect CPE (Q_D, refer to figure 2).

The reduction in R_S suggests the presence of shunt paths through combined defects $>10^4\times$ larger than combined defects in intact encapsulation films. Despite this large reduction, the electrolyte resistance R_E was not included in this model because impedance measurements were too large to resolve it within acceptable error. In contrast, failed *O-type* IDEs with bilayer encapsulation which exhibited catastrophic impedance decreases (refer to figure 4(c)) did require the inclusion of R_E (model not shown), emphasizing the effect of electrode openings on impedance. Correspondingly, the deliberate electrode exposure of f-UEAs required the inclusion of R_E of ~3 kΩ (figures 7(d)–(e)). The f-UEA impedance was predominantly characterized by the electrolyte resistance at frequencies >~1 kHz, and the ionic interactions at the electrode-fluid interfacial double layer, characterized with $n_C < 0.9$ (figure 7(d)). When observed, reductions in f-UEA impedance over time tended to occur at frequencies <100 Hz where the electrode impedance was highest. Figure 7(e) models a bilayer-coated f-UEA (6 μm parylene C thickness) that demonstrated a significant impedance decrease by study endpoint, fit using a circuit model employing a low R_S (2 versus 49 MΩ for figure 7(d)) and the addition of Q_D.

Of the parameters modeled, R_S best represented spectral behavior of failing devices over time, and was used to enable comparisons of bilayer and control failure dynamics across different devices. Figures 8(a)–(b) display changes in impedance spectra over time for failed bilayer and control *B-type* devices, respectively; these devices were removed from soaking on day 161 to permit failure analysis. Figures 8(d)–(e) plot the same information for failed e-UEA electrodes. The trends shown in these figures are representative of >90% of *B-type* and e-UEA failures. Both plots of bilayer impedance show clear evidence of protracted decreases in the spectra, with the bandwidth of these changes also increasing over time. In contrast, failed parylene devices display impedance decreases over much shorter durations of time, and changes occur over a narrower bandwidth confined to frequencies <200 Hz. We note that more rapid changes seen for control devices do not equate with changes ocurring earlier in time, else Weibull parameters for controls would indicate a tendency for early failure similar to bilayer devices. Plots of changing R_S over time (figures 8(c) and (f)) show that the impedance decrease of parylene-only samples occured within <10 d of study onset and stabilized. Surprisingly, both examples of failed control devices showed increasing R_S after

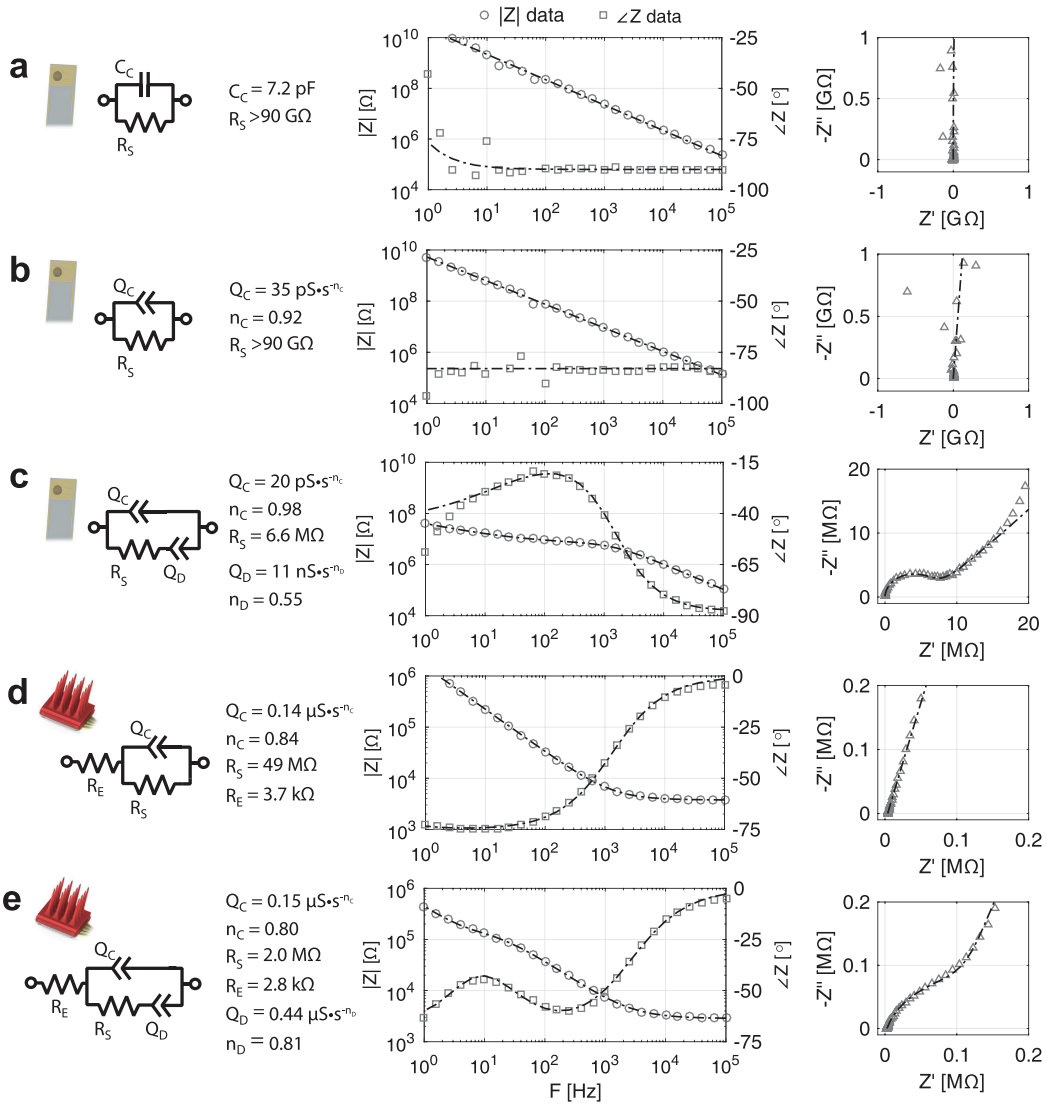

Figure 7. Circuit models and fits are shown for various devices, and for various states of encapsulation integrity. Device illustrations are shown for reference adjacent to the employed circuit model, next to which fitted parameters are specified. Center plots are of overlaid impedance magnitude and phase, and right-most plots are Nyquist diagrams. Plot markers show data, dotted lines represent circuit model fits. Goodness of fit values for modeled data were <0.1. Data modeled are from: (a) dry *B-type* IDE; (b) intact *B-type* IDE, taken from study endpoint; (c) failed *B-type* IDE (A + P encapsulation, note different phase and Nyquist axes scales), taken from study endpoint; (d) typical f-UEA; (e) f-UEA with impedance loss (A + P encapsulation, 6 μm parylene), taken from study endpoint (note different axes scales of f-UEAs from IDEs).

the initial fall to 23 MΩ and 90 MΩ, for *B-type* and e-UEA devices respectively. This is speculated to result from corrosion of electrode metal exposed by encapsulation defects. Both failed bilayer devices showed progressive reduction in R_S, beginning on day 75 for *B-type* and day 3 for e-UEA, which continued for >2 months. At study termination 79 d after first sign of R_S reduction, failed *B-type* R_S was 8 MΩ and did not appear to be progressing. Failed bilayer e-UEA displayed loss in R_S over the course of at least 230 d, at which point steady state appeared to have been reached around 8 MΩ as well.

Interestingly, the results of modeling R_S for f-UEAs corroborated well with *test structure* results. As previously shown, f-UEAs did not generally exhibit broad impedance reduction to the extent seen for *test structures*. However, decreases did occur in distinct instances, and spectral data presented in figures 10(g)–(h) are representative of these cases. Figure 8(g) is typical of two occurances of impedance decrease on one bilayer array, and figure 8(h) accurately depicts the slight decreases observed for all electrodes of the control UEA. The impedance decreases in these cases were smaller in magnitude

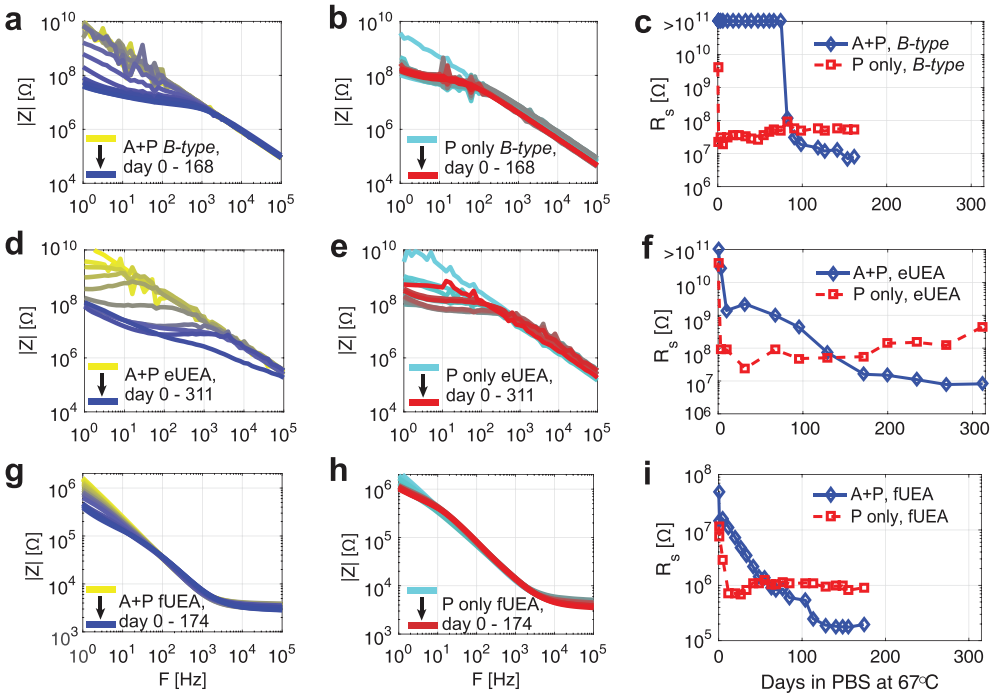

Figure 8. Changes in impedance magnitude over time for three different devices are depicted: (a)–(c) failed *B-type* IDE, (d)–(f) failed e-UEA, and (g)–(i) f-UEA with 6 μm parylene (note different *y*-axes). Progression of impedance loss is visualized for magnitude spectra of devices with (a)–(g) bilayer, A + P, and (b)–(h) parylene, P only, coatings, through color transitions of yellow to blue, and green to red, respectively. (c)–(i) The time course of impedance change is conveyed through plots of fitted R_S values for both encapsulation schemes, for each device type. Due to modeling limitations for high impedance elements, an R_S cap of 100 GΩ is imposed.

and more confined to frequencies <100 Hz compared to the same encapsulation on IDEs and e-UEAs. This is attributed to the significantly lower impedance of the deinsulated electrode tips. However, plots of R_S over time demonstrated patterns of shunt path evolution for bilayer and control devices similar to those observed for *test structures* (figure 8(i)), which was a rapid but confined R_S decrease for controls, versus a more gradual and exacerbated R_S decrease for bilayer devices. Specifically, R_S for controls decreased from 10 MΩ to a minimum value of 0.7 MΩ after 12 d, and slightly increased to steady state at 1 MΩ after 40 additional days of soaking. In contrast, reduction of bilayer R_S occurred from day 5 until day 128, beginning at 16 MΩ and ending at an apparent steady state value of 0.19 MΩ. While survival data indicated a varying degree of occurance for encapsulation failure effects across devices, these impedance and circuit modeling data point to common underlying mechanisms behind encapsulation failure for bilayer and control films, regardless of device type.

3.7 Post-failure analysis of e-UEAs and B-type IDEs

E-UEAs and *B-type* IDEs which exhibited leakage currents in excess of 1 μA were subject to copper electrodeposition to aid failure mode characterization. We did not pursue similar analysis of failed *O-type* IDEs because the presence of deliberate defects in *O-type* encapsulation rendered such analysis of little value, and failed *T-type* devices did not exhibit sufficiently large leakage currents for decoration. E-UEAs and *B-type* IDEs were also of particular interest due to their general manifestation of higher failure rates for bilayer devices compared to controls.

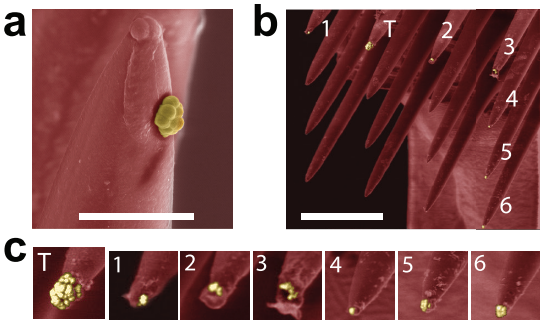

Figure 9. False color SEM images of failed e-UEA electrodes subject to copper electrodeposition after exhibiting high leakage current. (a) Copper deposit (yellow) on the side of single electrode tip, scale bar is 50 μm. (b) On an e-UEA with widespread failure, electrodeposition of a target electrode (T) was accompanied by deposition on six non-target electrodes, scale bar is 500 μm. (c) Detail of electrodeposition for tips shown in (b).

Copper accumulation on e-UEAs occurred at e-UEA tips, corresponding to the location of IrO_x tip metal (figure 9). In

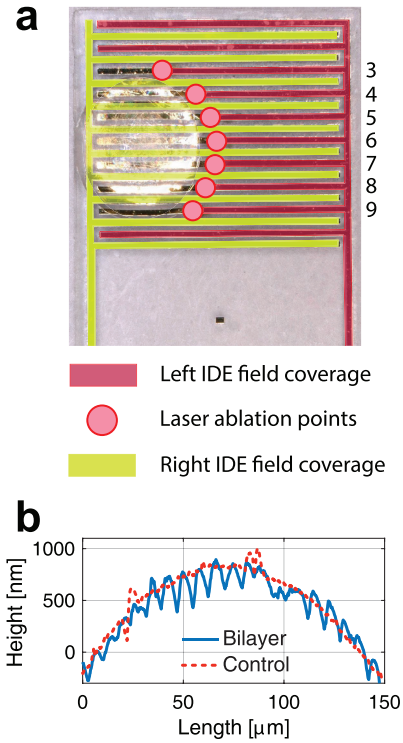

Figure 10. Post-failure analysis of failed *B-type* electrodes. (a) Schematic of laser ablation procedure to hide the region underneath silicone from EIS measurements. In this case, electrodes 3–9 from the right-most channel were ablated at points halfway or more down their length. (b) Profilometry of silicone coated with bilayer and parylene C control films.

some cases the deposition of a target e-UEA channel was accompanied by copper accumulation on adjacent channels that were not directly biased (figures 9(b)–(c)). Due to the high intrinsic electrochemical impedance of silicon, it is unlikely that such crosstalk was the result of shunt pathways formed between electrode channels on the tine side of the UEA, the surface of which is primarily silicon. Whereas electrode tips are separated by nearly 400 μm, gaps between backside bond pads are only 150 μm, making the backside a stronger candidate for the location of channel crosstalk pathways. The fact that all electrodeposited electrodes occupied a continuous path at the outer e-UEA edge suggests that electrolyte penetrated the encapsulation and seeped underneath the silicone, creating a continuous shunt path between the target electrode and other electrodeposited channels.

Surprisingly, failed *B-type* IDEs could not be copper decorated, as leakage currents to the external environment for these devices were not found to have sufficiently high current (<1 μA) to permit copper decoration. However, traditional leakage current measurements between IDE channels did surpass 1 μA levels, implying the leakage current paths were likely strictly underneath encapsulation. To determine if silicone over the IDE field played a role in this interfacial shunting, we laser ablated select IDE traces to remove the silicone region from EIS interrogation (figure 10(a)), and compared pre- and post ablation measurements. Impedances of the single failed control *B-type* IDE were restored post ablation to values similar to those of an intact device, however impedances of failed bilayer devices remained at pre-ablation levels. This suggests that for the failed *B-type* control, the leakage current path was likely confined to being underneath the silicone, while the shunt pathways for the bilayer devices originated and/or spread elsewhere.

To further understand how encapsulation integrity may be inflenced by the presence of silicone and similar materials, we employed optical microscopy and profilometry to characterize the silicone/bilayer surface. We consistently observed buckling on bilayer devices which had an amplitude of 200–250 nm and an approximate pitch of 8 μm, features which were absent on control device films (figure 10(b)). This buckling is attributed to the 120 °C deposition process for ALD alumina, after which cooling to room temperature incurs silicone contraction $>25\times$ that of alumina, due to thermal expansion coefficient mismatch (4 ppm °C^{-1} for ALD alumina [66] compared to >100 ppm °C^{-1} for silicone [67]). This buckling may have played a role in increasing the failure rate of *B-type* IDEs and e-UEAs with bilayer coatings compared to controls. While lower temperature ALD processes may mitigate this buckling and any associated detrimental effects, such processing could also increase the concentration of film defects [68]. Detailed study of the effects of this buckling and appropriate mitigating measures is a valuable topic for future work.

4. Discussion

4.1. Encapsulation failure mechanisms for test structures

Survival analysis using chronamperometry and characterization of encapsulation electrical properties using EIS were used to investigate the failure and mechanisms of our thin film encapsulation schemes. We tracked population lifetimes of 4 *test structure* device cohorts designed to model neural microelectrode features and topography, using 1 nA leakage current limit as a survival criterion. A Weibull distribution was found to best model the failure, suggesting that failure rate of *test structures* changes as a function of the power of time. For bilayer devices, the shape parameter (η) was >1, indicating a predisposition to infant mortality. In contrast, shape parameters for parylene-only controls had considerable variability suggesting a greater degree of randomness for their failures. We interpret this in conjunction with the other collected data to suggest that the ALD alumina coating introduced or exacerbated failure modes not present for control samples.

This interpretation is supported by EIS measurements of failed bilayer devices, which consistently demonstrated a larger decrease in impedance loss over a larger range of frequencies ($f < 10^4$ Hz) than control devices ($f < 100$ Hz). This has not been seen in prior works, which have shown impedance losses of failed IDEs (bilayer- and parylene only-coated) being confined to frequencies less than 100 Hz [29, 31]. However, this may be due to study limitations which terminate continuing data collection for devices that fail. This is

consistent with our experience that impedance <1 GΩ at 1 Hz correlates with leakage current >1 nA, and studies which terminate once this condition is met are not expected to show evidence of impedance loss at frequencies >100 Hz. In pursuing EIS measurements well past the time of failure, we uncovered encapsulation-specific patterns of impedance loss over time across devices. These patterns were identified through circuit modeling and tracking of the shunt resistance (R_S) parameter. Prior work has analyzed impedance change over time by tracking breakpoint frequency (−45° phase [25]), low frequency (0.1–1 Hz) impedance magnitude [69], and integral of the impedance curve [70]. However, the breakpoint frequency was not resolvable for the majority of figures 8(g)–(h) data, low-frequency impedances at later time points were less distinct than R_S for figure 8(d) data, and integral of the impedance curve does not readily lend itself to physical interpretation.

Tracking of impedance over time for failed devices revealed an asymptotic reduction in R_S for parylene controls that occurred over a period of days. In contrast, failed bilayer *test structures* demonstrated R_S reduction over the course of months. For both device types, which are representative of over 90% of such failures, this prolonged reduction resulted in R_S for failed bilayer devices that were at least 10× lower those of failed controls. The progressive decrease in this shunting resistance matches that observed for immersed parylene C-coated aluminum, fabricated to have poor interfacial adhesion [69]. The authors of this study attributed observed impedance reduction not to compromised bulk parylene C properties, but to delamination and ensuing direct exposure of the substrate surface to penetrated fluid and ionic species. Since we noted excellent parylene C adhesion to both ALD alumina-coated and -uncoated *test structures*, we attribute the progressive loss of impedance seen for failed bilayer-coated *test structures* to the breakdown of ALD alumina itself.

ALD alumina is known to undergo dissolution when exposed to 100% relative humidity [71], or direct contact with water, and this has been previously noted to be a possible failure mechanism driving impedance loss for bilayer-encapsulated devices [31]. Water penetration through parylene C defects to the ALD alumina material surface could lead to dissolution of alumina and undercutting of parylene C, increasing the defect size and further decreasing impedance. The kinetics of alumina dissolution would cause this impedance loss to occur at a slower rate than for failing parylene C controls. Controls would see rapid defect penetration and direct substrate exposure to the soak environment; however, the strong adhesion of parylene C to the substrate via adhesion promotor would arrest parylene C undercutting and defect growth. This would limit the area of the defect, correlating with a higher steady state impedance. These mechanisms are schematically illustrated in figure 11 and are consistent with impedance results for all devices. They also help to explain β shape parameter behavior for bilayer coatings and parylene controls. Bilayer coating failure rates could decrease over time as devices with parylene defects undergo fluid penetration, alumina dissolution, and defect growth to the extent that nearby electrode regions

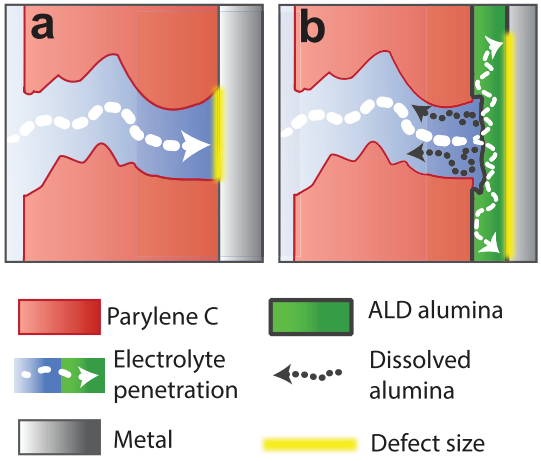

Figure 11. Illustration of encapsulation failure modes (not to scale). (a) Penetration through parylene defects is arrested near defect edge. (b) Defect penetration is followed by ALD alumina dissolution and defect growth.

are affected. Defects in ALD alumina films have been shown to increase in surface coverage when exposed to aging conditions [36]. This precedent for defect growth suggests parylene C defects located away from electrode areas would nevertheless affect electrode performance over time, if the parylene C were deposited on ALD alumina. In the case of parylene controls, since fluid penetration is limited to the immediate defect site, we expect device failure would only be noted if the parylene C defects were sufficiently close to electrode regions, closer than is required for the same failure to be noted for bilayer films. Thus, failure rates for controls are more dependent on the random localization of defects than for bilayer devices, and the variability of β for controls compared to bilayer devices reflects this. We expect that this variability would be tempered through increased sample sizes of control devices.

4.2. Impact of topography on test structures

ALD alumina and parylene C are attractive materials for dielectric coatings of devices with complex surfaces due to their conformal deposition. Both have been reliably shown to coat structures with high aspect ratios (AR) of ~10^3 [72, 73]. Accordingly, the topography that most affected *test structure* survival was not that of non-planar features, but that which deliberately introduced encapsulation defects (albeit away from measurement electrodes). For *O-type* IDEs to fail by way of the introduced defects, fluid penetration must sufficiently reach IDE digit traces located up to 25 μm away, a 4× longer distance than direct penetration through 6 μm-thick bulk film. Lifetimes of *O-type* IDEs were over 10× lower than all other *test structures*, which lacked such defects. This is consistent with prior studies showing failure propagation along a coating interface occurring much more rapidly than through bulk [69]. The encapsulation specific failure mechanisms illustrated in figure 11 are well

Table 3. Survival times for encapsulated devices tested under similar conditions, with various surface topography configurations.

Device type	Source	MTTF	Experimental temperature	MTTF at 37 °C (months)	MTTF ratio A + P:P	A + P versus P significance, test method ($p = 0.05$)
A + P, planar IDE	[29]	>9 months[a]	57 °C	>36[a]	>3:1	NA
P, planar IDE		3 months[a]	60 °C	12[a]		
A + P, planar IDE	[31]	214 d	57 °C	35	4.6:1	Yes, *t*-test
P, planar IDE		47 d	**67 °C**	8		
A + P, IDE w/coil[b]	[29]	5 months[a]		20[a]	5:1	NA
P, IDE w/coil[b]		1 month[a]		4[a]		
A + P, *T-type* IDE	**This work**	**450 d**		**120**	4.1:1	**No, log-rank test**
P, *T-type* IDE		**110 d**		**29**		
A + P, e-UEA		**510 d**		**130**	1:4.5	**Yes, log-rank test**
P, e-UEA		**2300 d**		**600**		

[a] Failure times taken from [29] were not statistically calculated MTTFs, but indications of minimum time before failure.
[b] See figure 2 for an illustration of coil topography.
NA—not available, no test performed.

represented by *O-type* impedance results (figure 4(c)), which show catastrophic EIS loss of failed bilayer coatings, and change to a much lesser degree for failed parylene controls.

O-type IDEs were designed to mimic exposed electrodes of neural interfaces, and these results suggest this feature to be a key vulnerability for encapsulation and impedance integrity. Care must be taken in neural electrode design to prevent encapsulation undercutting at electrode exposure sites from influencing neural electrode performance. Such measures may include sophisticated adhesion promotion strategies [25, 74], multilayer insulation such as oxide-nitride-oxide (ONO) underneath parylene C [75, 76], and electrodeposition coating of the electrode site which results in the occlusion of the insulation step-edge [77]. The ease with which ALD alumina is etched in solution compared to strategies such as ONO renders it a less effective choice for multilayer encapsulation.

Test structures which evaluated the integrity of conformal deposition in the presence of different topography and materials (laser ablations excluded) exhibited similar MTTFs between bilayer encapsulated groups, for this study. We tested topography-free IDEs (bilayer encapsulation) fabricated concurrently with both *T-type* and *B-type* devices, and did not find evidence of reduced MTTFs due to topography. Furthermore, our results do not indicate detrimental effects of topography when compared to lifetimes of previously tested planar IDEs, summarized in table 3 along with selected results from the present report. It is possible that the noted >2× change between lifetimes of IDEs tested at 57 °C without and with coil topography is due to random effects, which were not tempered by averaging owing to small sample sizes. Fused silica placement for *T-type* IDEs was designed in part to permit comparison to this prior topography study, and the bilayer-to-control MTTF ratio of 4.1:1 for *T-type* devices is in good agreement with corresponding ratios calculated from prior work. Since the advantage of bilayer coatings is best realized when failure risk is predominantly by way of penetration through bulk film, which is the case for planar coatings, it is apparent that *T-type* topography does not introduce additional failure mechanisms. This was consistent with previous results, given that *T-type* and coil topography was placed away from the IDE field, which is the region most sensitive to dielectric change. As such, the dielectric coatings over these regions were similar between these *test structures* and those without topography.

As seen in table 3, the MTTF for e-UEAs with parylene-only encapsulation is >4× larger than for bilayer samples, which is the reverse of that for *T-type* devices. *T-type* IDEs were designed in part to model the effects of electrode tine topography present on e-UEAs, and this discrepancy between *T-type* and e-UEA results suggests inadequate tine-model topography design, and/or the presence of e-UEA failure mechanisms in addition to those modeled by *T-type* devices. Copper deposition at the tips of failed e-UEAs imply that the sharp electrode tips themselves may be more predisposed to defect formation than anticipated by *T-type* IDEs, which employ a planar IDE electrode region. One possible cause of dielectric failure at tips is physical damage through handling, and *T-type* devices are largely immune to such handling damage, which may be a drawback to their design. In addition, it is also clear through e-UEA and *B-type* failure analysis that an additional risk of cross-channel shunting underneath silicone exists, and this may help account for the discrepancy between *T-type* and e-UEA results. However, according to our data, the inclusion of silicone underneath bilayer or parylene C encapsulation does not increase the likelihood of dielectric failure, evidenced by the much longer MTTFs of *B-type* devices compared to *T-type* devices. This is expected, as silicone is a widely used and capable water barrier material, and its coverage of the *B-type* IDE field in essence protects ~1/3 of the IDE from parylene C film defects.

4.3. Effects of encapsulation type on f-UEAs

F-UEA performance was not generally found to differ based on the presence or absence of ALD alumina. Devices with 6 μm parylene C thickness, with and without ALD alumina, demonstrated stable 1 kHz impedances of <10 kΩ for >3 years equivalent at 37 °C. These results are similar to other unreported UEA cohorts with and without bilayer encapsulation. In contrast, Xie *et al* found median 1 kHz impedance changes of -51% and +21% for UEAs with parylene C-only

and bilayer coatings, respectively, when soaked for 3 d in PBS at 37 °C [30]. This prior study concluded that the robustness of bilayer encapsulation permitted resolution of electrode metal degradation, indicated by increased impedance, which was otherwise hidden by the effects of defect formation in parylene C alone. However, it is equally possible that poor metal quality of the bilayer-coated UEA induced an effect opposite to that which was proposed, in that metal degradation may have hidden the effects of bilayer encapsulation breakdown. This breakdown would have been expected to occur more slowly than that for an array coated with parylene C alone, according to our data. This interpretation is consistent with the results of Xie *et al*, assuming metal stability on the control array was superior to that of the bilayer UEA. It is important to note that our study incorporated an electrode metal film re-engineered for improved stability, the details of which are saved for a later report. Thus, we no longer observe impedance increases for either encapsulation type. Unfortunately, the lack of full spectrum impedance from these prior results prohibits more detailed comparisons with our own. We affirm from our results that bilayer encapsulation has negligible, if any, beneficial effect on UEA stability compared to parylene C alone.

4.4. Extrapolation of test structure data to f-UEAs

One reason that evidence of encapsulation-specific impedance change was sparse for f-UEAs compared to *test structures* may be the low intrinsic f-UEA impedance of $<$10 kΩ at 1 kHz. Although fully encapsulated arrays (e-UEAs) which failed with the bilayer coating showed impedances universally lower than surviving e-UEAs, the average 1 kHz magnitude for these devices was still 100× higher than that of f-UEAs, at 1 MΩ. Additionally, shunting resistance (R_s) through encapsulation for failed e-UEAs rarely dropped below 10 MΩ. Shunt paths of such high impedance are not detectable at 1 kHz for our f-UEAs, but figures 8(g)–(h) shows examples of such shunting being evident at lower frequencies where intrinsic impedance is highest. There is a clear similarity between f-UEAs and *test structures* regarding the time course of shunt resistance decrease for both encapsulation schemes. Similar to *test structures*, the incidence of decreased impedances in f-UEAs is most exacerbated when encapsulation incorporates ALD alumina. The principle component analysis shown in figure 6 supports this, which detected the least amount of variance between f-UEAs and failed bilayer coated devices. Our interpretation is that undercutting of ALD alumina through parylene C defects or openings can give rise to shunt paths which infringe on microelectrode function, essentially through the undesired growth of accessible electrode surface area.

O-type device results suggest the electrode opening is a region vulnerable to dissolution of alumina, resulting in parylene undercutting and larger magnitude impedance decreases for f-UEAs. The plots of figures 8(g)–(h) support the presence of this mechanism. However, the prevalence and impact of this failure for *O-type* devices, and its rarity and smaller effect for f-UEAs are not consistent. One explanation may be that the nanoscale topography of iridium oxide metal at the bilayer deinsulation edge inhibits diffusion transport and dissolution, which proceeds along an unimpeded path for IDEs. This is consistent with previous observations we have made of ALD alumina etching in BOE, which tends progress on dendritic iridium oxide-coated substrates at less than half the rate of the same etching on polished silicon substrates. Another explanation is that although undercutting at the electrode tip exposes a path between electrode metal and parylene encapsulation for fluid ingress, the resistance through this narrow defect is still too high to have a measureable effect on electrode performance. However, devices which have multiple electrodes per shank could develop more significant cross-talk or parasitic pathways from this type of encapsulation degradation, as such undercutting would contribute to shunting between electrodes. In these cases, the encapsulation strategies mentioned in section 4.2 are especially appropriate.

Extrapolating from figure 8(i) data, a backside shunting resistance $R_S < 10$ MΩ is expected to decrease f-UEA electrode impedance at 1 Hz, and we anticipate that reducing the risk of this type of defect will improve neural electrode stability. As previously stated, f-UEA fabrication does not include bilayer/parylene C encapsulation of the backside silicone potting which protects the wire bond region, and increased backside shunt risk may arise from this limitation. We have undertaken preliminary efforts to develop fabrication schemes that permit continuous backside encapsulation, with *B-type* and e-UEA *test structures* designed in part to assess the value of such a modification. When coated with parylene alone, these devices exhibited shunt paths $>$10 MΩ even after failure, which occurred at $<$0.25× the failure rate of equivalent bilayer coated devices. This suggests that complete encapsulation of the UEA backside silicone with parylene C will have a beneficial effect on electrode stability. We reiterate here that failed control *B-type* shunting was confined to being between IDE traces underneath silicone, and provides a sound basis to draw conclusions concerning risks of inter-channel shunting and impedance loss.

4.5. Implications for in vivo applications

According to PCA data (figure 6) and 1 kHz statistical analysis of *test structures* (figure 4(e)), failure of parylene C encapsulation based on a rigorous leakage current criterion may not necessarily extrapolate to neural electrode instability. The same cannot be said of bilayer coated devices, which require defect-free parylene C (or other capping layer) if the ALD alumina film is not to become a liability. However, this difference in performance under the described *in vitro* conditions may not be so apparent for long-term *in vivo* applications. Physical damage to parylene C (cracking, thinning, cratering) has been historically observed over chronic *in vivo* time points [27, 64, 78], arising from aging mechanisms more complex than has been observed in temperature-accelerated Arrhenius reactions in PBS. Therefore, despite parylene C alone providing more stable performance than bilayer encapsulation according to our study, we do not advocate it as an ideal dielectric coating

for neural microelectrodes. Additional research is needed to uncover new materials and modifications that are suitable for implantable microdevices, and which provide robust protection *in vivo* over the long term. This may include modified fabrication procedures to reduce the degradation rate of ALD alumina towards the well regarded performance of bulk alumina, or evaluation of different materials utilizing the ALD technique. Furthermore, while a focus of this study was the evaluation of appropriate test substrates for implantable material investigations, equally important is the identification of test environments which can replicate aggressive *in vivo* aging mechanisms [79]. By bringing together advanced materials and robust testing techniques, novel microelectrodes can be developed which will cross the divide between the laboratory and the clinic.

5. Conclusion

Robust dielectric encapsulation films are needed for neural microelectrodes, to improve chronic *in vivo* stability over clinically relevant time points on the order of 10 years. In this work, we have developed a comprehensive experimental structure to examine novel materials and techniques for continued advancement of neural microelectrode technology. Innovative in our approach is the use of four novel *test structures* incorporating microelectrode features and topography, as well as functional Utah Electrode Arrays, to assess dielectric film performance.

Through *in vitro* accelerated aging at 67 °C in PBS, we used this experimental structure to evaluate a bilayer encapsulation scheme comprised of atomic layer deposited aluminum oxide and parylene C, in comparison to parylene C-only controls. Failure rates of devices and encapsulation schemes were assessed through survival analysis of *test structures* according to >1 nA leakage current failure criteria, while impedance measurements and circuit modeling revealed the extent of failures and how they occurred.

Our results indicate that the presence of openings in encapsulation (analogous to exposure of neural electrode sites) accelerate general encapsulation failure 10× compared to topographical features such as penetrating tines and silicone potting. These remaining topography types were not found to detrimentally affect encapsulation performance compared to lifetimes noted for simple planar *test structures*. A statistically significant difference in encapsulation lifetime was found for only 1 of 4 *test structure* device types according to the log-rank test, and MTTF of these devices coated with the bilayer was less than 0.25× that of controls. Impedance loss for failed devices with the bilayer coating was up to 100× that of failed parylene controls at 1 Hz, and impedance values for failed bilayer *test structures* were commonly below those of intact devices across the spectrum of 1–10^5 Hz. In contrast, failed parylene controls were typically indistinguishable from non-failed devices at frequencies >100 Hz. Circuit analysis of failed devices revealed that shunting resistances for failed parylene controls fell over a period of days and held. In contrast, failed bilayer devices underwent a progressive loss of impedance over the course of >2 months, and final values of shunt resistance were 10× lower than their control counterparts. Similar effects were noted in isolated incidents for functional microelectrode arrays with bilayer and parylene C encapsulation, but in general no performance difference was found between functional arrays coated with the bilayer and controls.

We surmise that the characteristics of *test structure* failure arose from fluid penetration of defects in parylene C, which was confined for control devices, but which dissolved ALD alumina and undercut bilayer encapsulation. Thus, the vulnerability of ALD alumina to water dissolution through parylene C defects compromises the benefits of its exceptionally low water vapor permeation rate for implantable electrode applications. Adjustments such as higher ALD process temperature may reduce ALD alumina impurities and tendency to undergo dissolution [68], and are worth considering in future studies. Additionally, other inorganic coating strategies like silicon carbide [18, 19] and ONO [80] may be more appropriately used for neural implant bilayer encapsulation, owing to their superior robustness in water compared to ALD alumina. Testing frameworks similar to that used in this report, which take into account the effects of neural electrode features and topographies, will be well suited to evaluate future encapsulation approaches. In this way dielectric coatings can be identified to improve the state-of-the-art for chronic neural electrode stability.

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CHAPTER 3

NEURAL ELECTRODE RESILIENCE AGAINST DIELECTRIC DAMAGE MAY BE IMPROVED BY USE OF HIGHLY DOPED SILICON AS A CONDUCTIVE MATERIAL

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Original research article

Neural electrode resilience against dielectric damage may be improved by use of highly doped silicon as a conductive material

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HIGHLIGHTS

- Doped silicon exhibits low bulk resistivity but high electrochemical impedance.
- Finite element models suggest use of silicon can improve neural electrode impedance stability.
- Reactive accelerated aging *in vitro* is used to evaluate electrode designs incorporating silicon.
- Impedance stability of neural electrodes can be improved by using silicon as a conductor material.

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ABSTRACT

Background: Dielectric damage occurring *in vivo* to neural electrodes, leading to conductive material exposure and impedance reduction over time, limits the functional lifetime and clinical viability of neuroprosthetics. We used silicon micromachined Utah Electrode Arrays (UEAs) with iridium oxide (IrO_x) tip metallization and parylene C dielectric encapsulation to understand the factors affecting device resilience and drive improvements.
New method: In vitro impedance measurements and finite element analyses were conducted to evaluate how exposed surface area of silicon and IrO_x affect UEA properties. Through an aggressive *in vitro* reactive accelerated aging (RAA) protocol, *in vivo* parylene degradation was simulated on UEAs to explore agreement with our models. Electrochemical properties of silicon and other common electrode materials were compared to help inform material choice in future neural electrode designs.
Results: Exposure of silicon on UEAs was found to primarily affect impedance at frequencies >1 kHz, while characteristics at 1 kHz and below were largely unchanged. Post-RAA impedance reduction of UEAs was mitigated in cases where dielectric damage was more likely to expose silicon instead of IrO_x. Silicon was found to have a per-area electrochemical impedance >10 × higher than many common electrode materials regardless of doping level and resistivity, making it best suited for use as a low-shunting conductor.
Comparison with existing methods: Non-semiconductor electrode materials commonly used in neural electrode design are more susceptible to shunting neural interface signals through dielectric defects, compared to highly doped silicon.
Conclusion: Strategic use of silicon and similar materials may increase neural electrode robustness against encapsulation failures.

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Abbreviations: UEA, Utah electrode array; IrO_x, iridium oxide; RAA, reactive accelerated aging; *Std*, standard electrode; *SiTip*, silicon tip electrode; *SiSh*, silicon shank electrode; *NM*, normal-metal electrode; *PM*, precise-metal electrode.

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1. Introduction

Implantable microelectrodes that record and stimulate neural signals have the potential to improve the quality of life for individuals with neural and motor disabilities, by enabling neuroprosthetic therapies (Ajiboye et al., 2012; Clark et al., 2014; Davis et al., 2016; Schwartz et al., 2006; Simeral et al., 2011; Wodlinger et al., 2014). However, clinical adoption of these technologies is hampered by inadequate functional lifetimes for neural electrodes (Polikov et al., 2005), which is attributed in part to the failure of dielectric encapsulation over time (Hämmerle et al., 2002; Ludwig et al., 2006; Seymour et al., 2009; Suner et al., 2005). These encapsulation materials include parylene C, polyimide, and silicon dielectrics such as silicon oxide, which have origins in integrated circuit (IC) manufacturing. The suitability of these materials to micromachining processes and conformal deposition on complex microstructures has motivated their use on neural interfaces. However, the aggressive *in vivo* environment presents challenges to material integrity not normally encountered in IC applications, resulting in failure modes that have been difficult to mitigate. Such failures are commonly accompanied by and detected through changes to electrode impedance and performance. Schmidt et al. evaluated parylene C-coated iridium microwires in primate cortex, and were among the first to correlate impedance reduction with dielectric damage and loss of single unit neural recordings (Schmidt et al., 1988). More recent studies have highlighted the tendency for parylene C to undergo cracking and damage *in vivo* (Barrese et al., 2016; Christie et al., 2016; Kane et al., 2013; Prasad et al., 2014). Additionally, polyimide receding and cracking (Prasad et al., 2012), as well as silicon oxide etching (Hämmerle et al., 2002), have been attributed to poor performance of implanted arrays. The stability of silicones and polyurethanes have been motivation for their use in the construction of macro-sized commercial neural interfaces such as cochlear implants and deep brain stimulation electrodes (Nazzaro et al., 2011; O'Malley et al., 2017), but these materials are difficult to apply to microelectrode construction. No microelectrode encapsulation material has been identified that can withstand 10 or more years exposure to the *in vivo* environment (Jorfi et al., 2015). This failing has motivated work to evaluate more robust encapsulation schemes, such as multilayer coatings (Han et al., 2012; Schmitt et al., 1999; Xie et al., 2014, 2013) and silicon carbide (Cogan et al., 2003).

The importance of intact dielectric coatings for penetrating microelectrodes is illustrated by Fig. 1, which models a neural electrode in tissue using equivalent circuits adapted from established work (Nelson et al., 2008; Robinson, 1968). We note that resistive and capacitive elements are simplified representations of complex behaviors which are functions of material properties, surface area, and electrolyte characteristics. In keeping with established convention, we utilize capitalized symbols to denote a bulk characteristic or behavior (*e.g.* resitance, capacitance), while lowercase symbols will be used to represent corresponding constituent properties (*e.g.* material resistivity, capacitance per unit area). Subscripts indicate the location of each component within the equivalent circuit and are always capitalized for readability. Fig. 1a shows that the extracellular neural voltage signal V_T is amplified to a recorded output V_{REC} after being conducted through physiological media with the associated spreading resistance (analogous to electrolyte solution resistance) R_S, across electrode impedance comprised of C_E and R_E, and through resistance R_M of the current conductor (*e.g.* a shank or metal trace). The presence of parasitic shunting capacitance C_P (across electrode encapsulation) as well as amplifier input impedance Z_A can cause current to leak to ground or the local environment. To obtain a V_{REC} with high signal-to-noise ratio (SNR), it is commonly understood that the impedance from neuron to amplifier should be as low as possible

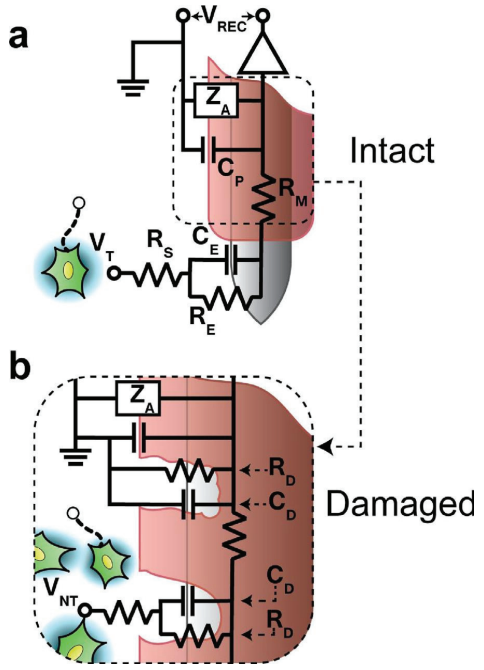

Fig. 1. (a) A sound dielectric coating on a neural electrode exhibits very small parasitic capacitance C_P and creates a single electrical path from the target neuron to recording hardware. Remaining symbols: V_T – voltage signal of target cell; R_S – tissue spreading resistance; R_E, C_E – electrode faradaic resistance and double layer capacitance; R_M – resistance of the current conductor; Z_A – amplifier input impedance; V_{REC} – recorded voltage. (b) Insulation damage creates undesired current pathways, which may introduce biological noise from non-target cells or shunt electrical signal to the local environment. Symbols: V_{NT} – voltage from non-target cells; R_D, C_D – resistance and capacitance of surfaces exposed by encapsulation damage.

(Cui and Martin, 2003; Nelson et al., 2008), in part to reduce thermal Johnson noise (Sharma et al., 2016). For stimulation applications, lower electrode impedance also correlates to higher allowable charge injection within safe voltage limits (Brummer and Turner, 1977; Cogan et al., 2016). Amplifier input impedance should be very high (>10 GΩ) to minimize current flow to the amplifier and decrease the electrical load from the recording circuit. Dielectric coating material is chosen to minimize parasitic capacitance (*e.g.* <10 pF). If encapsulation damage creates resistive and capacitive defect pathways to the current conductor (R_D and C_D in Fig. 1b), the recorded voltage may be confounded by biological noise V_{NT} from non-target cells (Hughes et al., 2000; Lempka et al., 2011), as well as reduced in amplitude through low impedance shunting pathways to the local environment. These same shunt pathways may also redirect stimulation current to non-target regions, reducing stimulation efficacy.

Let us consider the specific material characteristics that drive surface area-integrated behaviors. The model in Fig. 1 suggests that electrode architectures which do not differentiate electrode and conductor (causing r_D and c_D to be equal to r_E and c_E, respectively) may be highly vulnerable to performance loss from encapsulation damage. Use of the same material for electrode site and as the conductor is typical of microwire-type architectures, for which the penetrating assembly and electrode site are of tungsten (Patrick et al., 2011; Prasad et al., 2012), iridium (Schmidt et al., 1988, 1976), or platinum/iridium (Prasad et al., 2014). For these device types, encapsulation defects, in essence, create new

electrode sites equally capable of transferring charge with the physiological environment as the original electrode, albeit in a manner likely to introduce biological noise to recordings, or divert stimulation pulses.

As a different case, we can consider a neural interface constructed of two distinct conductive materials: one material with low electrochemical impedance (combined impedance of double layer capacitance and charge transfer resistance) for the electrodes, and a second material with low *electronic* impedance but high electrochemical impedance for the current conducting shank or trace. Compared to the single-material electrode, the vulnerability of such a device to negative effects arising from encapsulation degradation might be decreased, as encapsulation degradation over the current conductor region would only introduce shunting pathways of high impedance compared to the original electrode site. Therefore, flow of charge between the original electrode and tissue would remain the predominant current path. While it is noted that such architectures may introduce interfacial contact impedance between the electrode and conductor materials, this impedance is negligible compared to that of the electrode/electrolyte interface for well-designed devices.

Material coatings with low electrochemical impedance to improve charge flow at the biotic-abiotic interface have been investigated by several groups, and include iridium oxide (IrO_x) (Cogan et al., 2004; Han and McCreery, 2008; Kane et al., 2011; Weiland and Anderson, 2000), PEDOT (Cui and Martin, 2003; Ludwig et al., 2011, 2006), and carbon nanotubes (Baranauskas et al., 2011; Jan et al., 2009; Lovat et al., 2005). These coatings are used to lower the impedance of electrode architectures comprised of more common conductive materials such as iridium and gold, and the change can be an order of magnitude or more (Han and McCreery, 2008; Kozai et al., 2012; Wilks et al., 2009). As previously described, a potential side effect of these paradigms is the reduction of sensitivity to dielectric defect formation over the conductive (non-electrode) path. Since specific impedance associated with r_D and c_D could be up to 10× greater than that of the electrode region in such cases, these architectures could be expected to have a higher tolerance for dielectric degradation compared to monolithic electrodes. Further extending this concept leads to the possibility of electrode architectures comprised of conductive materials chosen specifically for their poor charge transfer characteristics and high interfacial impedance with physiological electrolytes. That is, a consideration of neural electrode design can be the selection of conductive materials which pass charge easily within their bulk and across solid material junctures (*e.g.* metal), but poorly through electrochemical interfaces. The use of low-impedance electrode coatings with conductive materials that have both suitably low r_M, and high electrochemical impedance, could strengthen neural electrode robustness against degradation to the dielectric coatings. From work with the silicon micromachined Utah Electrode Array (UEA), we have found the per-area electrochemical impedance of highly-doped silicon to be up to 1000× higher than IrO_x, making the UEA an appropriate device to evaluate this hypothesis.

The UEA is distinct among neural electrode technologies for its use of doped silicon as both an architectural material, as well as the conducting pathway between electrodes and external hardware adapters. Discussion regarding use of silicon in fabrication of the UEA has focused the development of the fabrication process, and its utility as a micromachining substrate (Branner et al., 2001; Lee et al., 2005; Wark et al., 2013). Since its inception, metal coatings on the silicon tips have been required to attain functionally useful charge transfer between silicon and tissue. However, optimization of metallization processes has focused on ease of manufacturability, without regard to how the resulting architecture influences device resilience to encapsulation damage. No published work has been reported to identify and characterize the electrochemical properties of silicon as part of more comprehensive efforts to model neural electrodes and their degradation modes. Furthermore, little consideration to the silicon doping concentration for UEAs has been given since the first investigations revealed that *p*-type silicon of 0.01–0.05 Ω cm resistivity was sufficient for the neural electrode applications of the time (Jones et al., 1992).

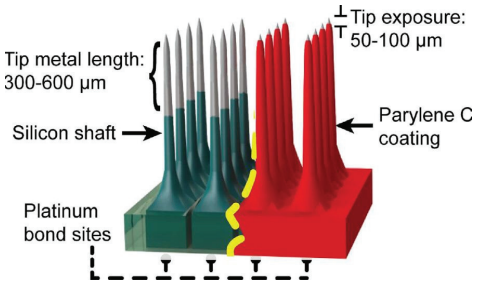

Fig. 2. A diagram of a standard UEA shows silicon in blue-green, IrO_x in gray, and parylene C in red. The dashed yellow line delineates pre- and post-encapsulation processing, and is used to better illustrate the structure of UEA. The silicon and tip metal geometry of the UEA before parylene C encapsulation is illustrated to the left of the yellow line, to the right represents post-encapsulation and tip exposure. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Utilizing the UEA, this report explores the impact of material choice and fabrication strategy on microelectrode impedance, and scrutinizes how silicon may be used to enhance resilience against degradation of the dielectric coating. First, we characterize the electrochemical impedance of the UEA as defined by parameterized surface area exposure of particular materials, to identify how exposure of silicon and IrO_x electrode metal result in impedance changes from ideal devices. Finite element modeling is used to confirm our understanding of surface-area specific impedance behaviors. Next, we used an aggressive *in vitro* stress test, reactive accelerated aging (RAA), to simulate chronic implantation and associated material degradation of UEAs. Employing this method, we investigate if the high electrochemical impedance of silicon can reduce the magnitude of impedance change that accompanies encapsulation damage *in vivo*. Finally, we report the electrochemical characterization of silicon with different doping types and concentrations compared to other microelectrode materials in common use, to advance our understanding of the contribution silicon can make as a component of neural electrodes.

2. Material and methods

We utilized three different fabrication approaches to characterize UEA material impedances, and these approaches deviated by varying degrees from standard UEA processes. To avoid repetition, Section 2.1 outlines the standard UEA fabrication procedure, with Fig. 2 illustrating the key accompanying features of a baseline UEA. Sections 2.1.1–2.1.3 describe how the standard process was modified per the needs of our three investigational approaches. Our characterization efforts also employed planar test electrodes, whose fabrication and characterization methods are described in Section 2.5.

2.1. Standard UEA fabrication

UEA fabrication has been previously reported (Bhandari et al., 2010; Jones et al., 1992; Rousche and Normann, 1998). Briefly, UEAs for this study were micromachined from *p*-type boron-doped silicon (0.01–0.05 Ω cm, Virginia Semiconductor, Fredericksburg, VA),

which was diced, processed and etched to create 4 × 4 arrays of sharp tines 1 mm in length, electrically isolated by glass-filled kerfs (N = 16 electrodes per array). Platinum contact pads were sputter deposited on the array backside, and annealed at 375 °C for 45 min in ultra-high purity forming gas, to form Ohmic contacts to the electrodes for wire bonding. The electrode tip metal deposition procedure began with UEA cleaning in buffered oxide etch (BOE) (Transene, Danvers, MA) for six minutes, followed by a DI water rinse and packaging in aluminum foil such that only a desired length of electrode shank was revealed through the foil. For standard production, this length is typically not precisely controlled and ranges from 300 to 600 μm. Iridium oxide (IrO_x) with a thickness >600 nm was reactively sputtered on revealed shanks, then annealed in pure oxygen at 475 °C for 30 min after removing the foil, to form a mechanically robust Ohmic contact between the silicon and tip metal (Negi et al., 2009; Yoo et al., 2012). Encapsulation in parylene C followed tip metal processing. To enhance parylene C adhesion, UEAs were first exposed to vapor-phase A-174 silane adhesion promoter (Momentive Performance Materials, Waterford, NY) for two hours in a vacuum desiccator. A 6 μm thick film of parylene C was deposited from DPX-C dimer in a PDS 2010 (both from Specialty Coating Systems, Indianapolis, IN). Arrays were placed in a second aluminum foil mask and etched in oxygen plasma to create desired tip exposure lengths through parylene C encapsulation. The second foil masking step is controlled more precisely than the first masking procedure for tip metal length, and this exposure was 50–100 μm for our devices. Thus, an IrO_x length of up to 550 μm remained unexposed underneath parylene C. The 50–100 μm exposure range was greater than the tip exposure range of 40–60 μm for UEAs commercially fabricated by Blackrock Microsystems, and the larger surface area of our arrays was one factor contributing to reduced baseline UEA impedances compared to those of previous reports. The larger exposure range arose from 4 × 4 UEA manufacturing limitations that were discovered during the course of this study, but as it did not confound the trends we sought to characterize it was deemed acceptable for our needs. Further processing, such as UEA wiring to external connectors, only proceeded according to the requirements of our three approaches outlined in the subsections that follow.

2.1.1. UEAs with parameterized material exposure

To understand how the use of silicon in UEA fabrication can influence electrode impedance and changes in the impedance due to encapsulation degradation, our first investigational approach characterized UEAs with parameterized exposures of IrO_x and silicon. The parameterization strategy included representations of worst-case scenarios for UEA material damage. These scenarios reflected complete removal of dielectric encapsulation or electrode tip metal, and all combinations thereof, and are listed in Table 1 with their associated UEA parameters as well as nomenclature to be used in the remainder of this report. One 4 × 4 UEA of each style was made and characterized specifically for this study (the reader is referred to Fig. 7a in Results and discussion for device images). The justification for all styles is evident save for the precise metal/*PM* UEA, which was distinguished by a deviation from typical array processing in that IrO_x was deposited to a tip length of only 50–100 μm, rather than the standard 300–600 μm. The *PM* UEA was designed to help us evaluate our hypothesis that the high electrochemical impedance of silicon causes its contribution to the impedance spectrum to be largely negligible, and that this can be exploited in device design to improve robustness. Since *PM* electrodes lacked parylene C encapsulation but otherwise exhibited similar exposed IrO_x geometric surface areas as those of standard/*Std* electrodes, a high degree of similarity between *PM* and *Std* impedance spectra would support our hypothesis.

2.1.2. UEAs for model validation

We developed a finite element model of UEA electrode architecture in saline, described in Section 2.4. This model permitted exploration of the effects that exposed silicon (through encapsulation damage) affected impedance characteristics. To validate this model, our second investigational approach utilized a 4 × 4 Utah Slanted Electrode Array (USEA) which had electrode shank lengths that varied by row and increased linearly from 0.7 to 1 mm. All shanks were coated with precise/*PM*-style tip metal, with target tip lengths of 50–100 μm. For tip exposure, the array was inserted through foil such that the back (bond pad) side of the USEA was parallel to the foil plane, creating tip exposures that varied from 65 μm for the shortest shanks, to 335 μm for the longest shanks. Etching in oxygen plasma removed the desired parylene C lengths and created a USEA with consistent electrode tip lengths but differing silicon exposures, against which we validated our model.

2.1.3. UEAs for reactive accelerated aging

Two UEA cohorts, one control and one experimental group, were fabricated for our third investigational approach which employed an aggressive RAA study. Control UEAs were designed to mimic the standard/*Std* UEA design, utilizing a conservative target tip metallization length of approximately 300 μm. Parylene C encapsulation and tip exposure followed standard processes. A micrometer was used during aluminum foil mask preparation for tip metal and exposure processes to facilitate reliable and repeatable lengths, which were verified using scanning electron microscopy (SEM). UEAs were manually wire bonded (West Bond, Anaheim, CA) to custom gold-flashed printed circuit boards (PCBs) (Circuit Graphics, Salt Lake City, UT) using polyester enamel-insulated gold (99% Au:1% Pd) bonding wire (Sandvik, Stockholm, Sweden). Bond pads and wire were over coated with MED-4211 silicone (NuSil, Carpenteria, CA).

The experimental UEA cohort differed from controls only in tip metal length, which was targeted near 100 μm, mimicking that of the precise metal/*PM* UEA. The metal length for the experimental group was chosen to better match tip exposure length compared to controls while being slightly longer than typical tip exposure length. This was done to reduce the likelihood that silicon would be revealed from beneath parylene C after oxygen plasma processing of experimental UEAs, in order to ensure matching initial conditions for experimental and control cohorts. Illustrations of control and experimental electrodes are given in Fig. 3.

2.2. Reactive accelerated aging

Aging of the UEAs described in Section 2.1.3 was performed in a reactive accelerated aging (RAA) system developed by Takmakov and associates (Takmakov et al., 2015), which exposes devices to a solution of 20 mM H_2O_2 as an oxidizer in phosphate buffered saline (PBS) at 87 °C. Aging occurred in a jacketed flask (Pine Research Instrumentation, Durham, NC) which was temperature controlled using a Haake C-25 recirculating heater with mineral oil (Fisher Scientific, Pittsburgh, PA). RAA aging for seven days has been reported to cause impedance reductions for UEAs, as well as Michigan-style probes, microwire arrays, and floating electrode arrays, therefore we aged our devices for seven days to be consistent with prior work (Takmakov et al., 2015). The half-life of H_2O_2 is approximately 20–30 min at 87 °C, therefore the target concentration was maintained through timed pumping of H_2O_2 refill and waste. Concentration was monitored *via* direct measurement of hydrogen peroxide adsorption in UV at 240 nm using offline UV–vis spectrophotometry (Ocean Optics, Dunedin, FL). System measurements were compared to a 20 mM reference sample, and did not deviate more than 3 mM from the targeted value throughout the experiment duration.

Table 1
UEAs with parametric material exposure.

Electrode style	Acronym	Description			Representative damage scenario
		Parylene C	IrO_x tip length	Tip exposure[a]	
Standard UEA	*Std*	Yes	300–600 μm	50–100 μm	•Ideal undamaged scenario
Silicon tip	*SiTip*	Yes	None	50–100 μm	•Damage to IrO_x electrode metal
Silicon shank	*SiSh*	None	None	NA	•Destruction of IrO_x and dielectric coating, complete Si exposure
Normal metal	*NM*	None	300–600 μm	NA	•Destruction of dielectric coating, full IrO_x and Si exposure
Precise metal	*PM*	None	50–100 μm	NA	•**Special case**: dielectric damage with **reduced** IrO_x exposure

[a] Tip exposure refers to tip length exposed through parylene C, and thus was not applicable to designs lacking parylene C.

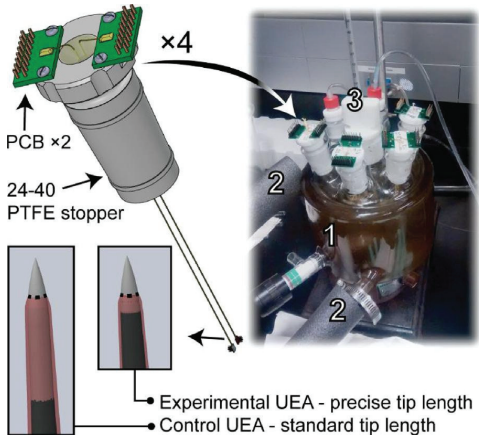

Fig. 3. A model of the UEA-stopper assembly (left) is shown with one experimental and one control UEA mounted, such that PCBs are not exposed to the RAA bath. Electrode detail illustrates tip metal length difference between experimental and control UEAs, dashed lines denote tip exposure through parylene C (shown semi-transparent). Silicone filled the through hole where UEA wire bundles passed to limit evaporative loss of RAA solution. Four such assemblies were incorporated into the RAA flask (right), shown with evacuation port for the inner PBS+H_2O_2 aging chamber (**1**), insulated ports for recirculation of heated bath oil through the outer heat-transfer jacket (**2**), and connections for thermometer, refill pump and waste pump (**3**).

To permit UEA aging while preventing PCB damage and associated impedance artifacts, UEAs were mounted in custom machined 24/40 PTFE flask stoppers for integration into the RAA system (Fig. 3). One control UEA and one experimental UEA were integrated in each stopper, and four stoppers were used for a total of N = 4 UEAs per cohort. Pre- and post-RAA characterization was carried out using electrochemical impedance spectroscopy (EIS) and backscattered imaging mode in a scanning electron microscope (BSEM) (FEI, Hillsboro, OR). EIS detected changes to the electrochemical performance of UEAs, while BSEM permitted identification of UEA materials and associated changes through Z-contrast imaging.

2.3. Electrochemical characterization of UEAs

EIS is a standard technique for evaluating electrochemical performance (Cogan, 2008; Gunalan et al., 2009; Merrill and Tresco, 2005), and changes in EIS from as-fabricated values can reflect degradation of electrode or encapsulation materials. The UEAs in this study were characterized *via* two-electrode EIS utilizing a large platinum wire (>24 mm^2) as both counter and reference electrode. Measurements were conducted over five decades from 1 to 10^5 Hz at 10 points per decade, with a Reference 600 potentiostat (Gamry Instruments, Warminster, PA) utilizing a 25 mV RMS excitation signal. Equivalent circuit curve fitting to find characteristic electrode parameters was performed with Gamry Echem Analyst utilizing

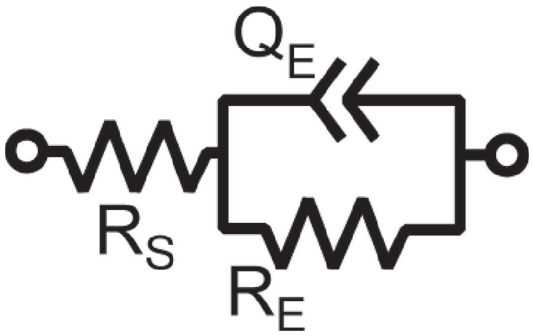

Fig. 4. Equivalent circuit of UEA electrode in PBS, used for electrochemical modeling and parameter fitting. R_S is spreading resistance through solution, R_E is charge transfer resistance at the electrode-electrolyte interface, and Q_E is imperfect capacitance (replacing C_E in Fig. 1a) at the electrode interface.

the simplex algorithm. Impedance curves were fitted to a modified Randles circuit (Randles, 1947) presented in Fig. 4, where R_S is spreading resistance through electrolyte, R_E is electrode charge transfer resistance, and Q_E is a constant phase element (CPE) modeling imperfect capacitance at the electrode/electrolyte interface. The CPE is defined as

$$Z_{CPE}(\omega) = \frac{1}{Q_0(j\omega)^n},$$

where Q_0 is CPE admittance at a frequency of 1 rad/s in units of S s^{-n}, j is the imaginary number, ω is frequency in rad/s, and n is a value between 0 and 1, describing characteristics between resistive and capacitive behavior, respectively. The overall equation for fitting EIS data to find electrode parameters was therefore:

$$Z_{electrode,EIS}(\omega) = R_B + \frac{R_E}{1 + R_E Q_0 (j\omega)^n}.$$

The electrolyte solution used to evaluate impedances was PBS, prepared with 140 mM NaCl, 2.6 mM KCl, 1.8 mM KH_2PO_4, and 10 mM Na_2HPO_4. Arrays from Section 2.1.3 were measured in PBS directly. In contrast, to focus on EIS contributions of the penetrating electrode architecture, measurements of arrays from Sections 2.1.1 and 2.1.2 were performed in PBS-agar. This eliminated UEA backside or wire bond contributions to impedance measurements, as only penetrating electrodes were pressed into agar. Agar was prepared by mixing PBS with 2-hydroxyethyl agarose (Sigma Aldrich, St. Louis, MO) at 150 °C, and allowing the mixture to cool and gel. Impedance measurements taken using agar and PBS alone verified that any differences due to medium were indiscernible.

2.4. Finite element analysis

We used finite element analysis (FEA) to model electrode impedance and refine our understanding of how material surface area affects impedance, particularly with regard to the UEAs

described in Sections 2.1.1 and 2.1.2. The FEA simulations were performed in COMSOL 5.2a (COMSOL Inc., Los Angeles, CA) utilizing the current conservation module in the frequency domain. Current conservation was chosen rather than an electrochemical interactions approach because modeling the complex charge and mass transfer kinetics that occur at the electrode/electrolyte interface was outside the scope of our study. Our simplified approach modeled electrode impedance as an equivalent circuit similar to Fig. 4, modified to be a function of fitted material parameters, surface area, and three dimensional geometry. According to the COMSOL 5.2 AC/DC Module User's Guide, the current conservation module solves for the continuity equation

$$\nabla \cdot J = I_j,$$

where I_j is a current source and J is current density as given by the continuum form of Ohm's Law

$$J = (\sigma + j\omega\varepsilon_0\varepsilon_r)E + J_e\,.$$

For (4), σ is material conductance, ε_0 is vacuum permittivity, ε_r is material relative permittivity, E is electric field, and J_e is external current density contribution. To account for imperfect electrode/electrolyte interfacial capacitance that arises from complex electrochemical interactions, contact impedance domains were employed which approximated the net effect of these interactions. The use of contact impedance domains also eliminated the need to model very thin metal films, which was beyond the scope and computational resources available. The contact impedance modifies a domain boundary to have parallel resistor-capacitor characteristics, and adjusts the current density-voltage relationship according to (5)

$$\vec{n} \cdot J = \left(\frac{1}{\rho} + j\omega c\right)\Delta V,$$

where $\vec{n}$ is the outward normal to the surface (not to be confused with CPE parameter n), ρ is surface resistivity, c is area-specific capacitance, and ΔV is the voltage differential across the boundary. From expansion of (1) and equating to parallel RC circuit impedance, it can be shown that CPE impedance matches RC behavior according to frequency-dependent RC parameters (6), (7):

$$R_{CPE}(\omega) = \frac{1}{Q_0 * \omega^n \cos\left(\pi * \frac{n}{2}\right)}$$

$$C_{CPE}(\omega) = Q_0 * \omega^{n-1} \sin\left(\pi * \frac{n}{2}\right)\,.$$

R_{CPE} and C_{CPE} parameters for IrO_x and silicon were calculated using Q_0 and n derived from EIS and equivalent circuit fitting. Normalization of Q_0 to estimated material surface area permitted approximation of ρ and c in likewise manner. In this way the CPE-like behaviors of IrO_x and silicon surfaces exposed to PBS were modeled through contact impedance domains. However, this method did not account for the effect of charge transfer resistance R_E (Fig. 4). The purpose of our FEA technique was to strengthen our understanding of surface area-dependent and material-dependent impedance trends, which are most strongly tied to the CPE characteristics of electrodes. Furthermore, we have found that R_E values often exceed the impedance magnitude ranges reported for UEA electrodes across 1–10^5 Hz, and R_E tends to have little influence on impedance fitting at frequencies >100 Hz. Given that the most commonly used characteristic frequency for electrode impedance is 1000 Hz, the anticipated error from R_E omission was acceptable.

A schematic of the finite element model is shown in Fig. 5. A three dimensional representation of an electrode was made in SolidWorks (Dassault Systèmes, France) based on measured UEA dimensions, and was imported into COMSOL as the basis for the FEA model. Variable height partitions were added which divided the surface of the model into multiple boundaries that could be assigned to IrO_x, silicon, or parylene C characteristics. IrO_x and silicon behaviors were accounted for by using the contact impedance method previously described. Various model simplifications were employed to minimize computational burden after confirming negligible (<5% maximum) effects on edge cases; these simplifications included representing the parylene C coating as perfectly insulating, the use of a single lone electrode rather than one surrounded by eight others, and limiting PBS domain geometry to a cylinder of 5 mm height and radius. PBS resistivity was 62.5 Ω cm, based on values available from vendors of premixed PBS tablets, while the electrode solid domain was assigned the median silicon resistivity reported by vendors (0.025 Ω cm). PBS cylinder sidewall boundaries were assigned as floating potentials. Ground was assigned to the PBS boundary opposite the electrode, while the electrode back side was assigned as a terminal. All other faces were insulating. Frequency domain calculations were made from 1 to 10^5 Hz at three points per decade.

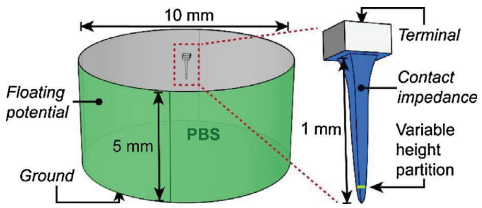

Fig. 5. A single electrode tine in PBS (cylinder) was modeled for FEA calculations. PBS container sidewalls (green) were floating, and the bottom boundary was assigned as ground. Variable height partitions divided the electrode model surface into multiple boundaries according to varying tip length and exposure conditions. The electrode surface boundaries shown in blue were assigned contact impedance characteristics of IrO_x or Si, or were insulating to represent parylene C, depending on the electrode design under investigation. The electrode backside was the model terminal. All other regions shown in gray were always insulated. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

2.5. Planar electrode fabrication and characterization

We fabricated planar electrodes to compare the electrochemical properties of silicon to those of other common materials used in neural electrode construction (Lee et al., 2016). Electrodes were constructed utilizing boron-doped *p*-type silicon of 1–20 Ω cm, 0.01–0.05 Ω cm (substrates used for UEA fabrication), and 0.001–0.005 Ω cm, as well as arsenic-doped *n*-type silicon of 0.001–0.005 Ω cm resistivity (University Wafer, South Boston, MA). The 0.001–0.005 Ω cm silicon was chosen in part to compare to carbon fiber electrodes of similar resistivity (Kozai et al., 2012). Measurements from *n*-type silicon were performed to elucidate any difference in the electrochemical properties of the interface associated with the different carrier type and the associated changes in Fermi energy (or chemical potential). Impedances of these silicon materials were compared to those of iridium oxide, iridium, platinum, tungsten, and gold metals.

Planar silicon electrodes (Fig. 6a) were fabricated by sputter deposition of platinum and iridium, followed by liftoff to expose octagonal silicon areas of 0.81 mm^2. Ohmic contact between metal and silicon was created through annealing at 375 °C as described in Section 2.1. Photolithography followed to carefully insulate all but 0.53 mm^2 hexagonal areas over silicon. This was the final electrode surface area for silicon electrodes, as well as metal electrodes which were also sputter deposited and lithographically patterned (Fig. 6b). This relatively large area, compared to that of UEA electrodes in this study (0.007–0.01 mm^2 for tip exposures of

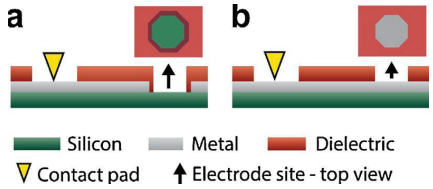

Fig. 6. Cross-sectional schematic illustrations of planar electrodes for measuring material impedance (not to scale). (a) Silicon electrodes were fabricated with an iridium base metal layer to minimize the impact of silicon bulk conductivity on electrochemical measurements. A platinum adhesion layer between iridium and silicon permitted formation of platinum silicide and an Ohmic contact between iridium and silicon. (b) Five types of metal electrodes were fabricated, utilizing iridium oxide, iridium, gold, platinum, and tungsten.

80–100 μm), was necessary to permit resolution of spreading resistance for silicon electrodes within the measured frequency range. This spreading resistance was not readily resolved for a silicon electrode with surface area similar to UEA electrodes, as the innate impedance of the smaller silicon electrode interface was too large. Spreading resistance was expected to be shared across electrodes of different materials if similar electrode geometries and measurement configurations are employed, and was therefore valuable for ensuring that our comparisons between materials were sound.

EIS spectra from planar devices were collected in PBS, using a three-electrode configuration including an Ag/AgCl reference electrode (Beckman Coulter, Brea, CA) and platinum wire counter electrode (>24 mm^2). The three-electrode configuration was chosen to ensure the most stable and accurate measures of high-resistivity silicon impedance. Electrodes were measured with a Gamry Reference 600 as described in Section 2.3. Based on intra-cohort variability, between three and six measurements were averaged per electrode material. Despite careful surface cleaning and processing to approximate silicon surface conditions of UEA tines, sample sizes of N > 3 were particularly needed for planar silicon devices to derive average values representing group convergence.

3. Results and discussion

3.1. EIS of parametric UEA material exposure

To evaluate the effect of exposed silicon surface area on UEA impedance, we fabricated five UEA styles with parameterized material exposure and N = 16 electrodes each. These devices represented electrodes with intact and degraded parylene encapsulation, and a summary of electrode characteristics for each device is given in Table 2. Arithmetic means and standard deviations (SD) for electrode tip lengths were calculated from SEM micrograph measurements. Representative SEM images presented in Fig. 7a and show each device type. Devices in Fig. 7a are shown in descending order according to 1 kHz impedance, for convenient visual reference to measurements shown in Fig. 7b. Surface areas were

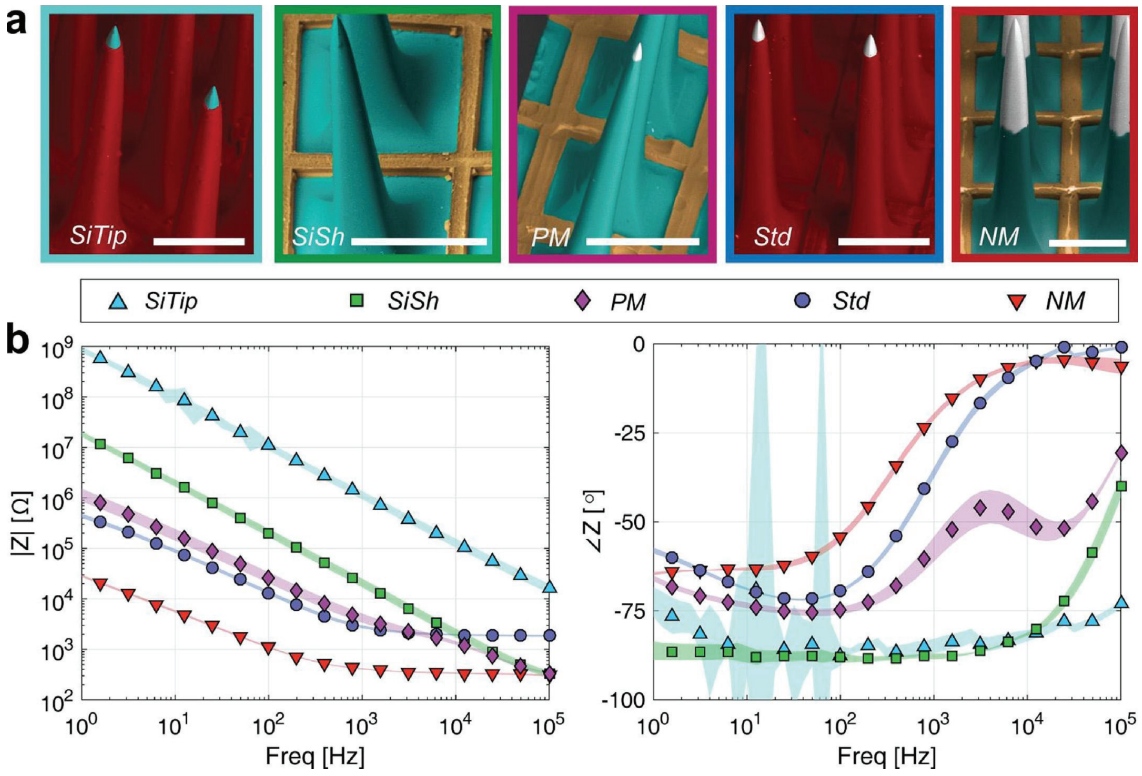

Fig. 7. (a) Representative SEM images of devices used to measure parametric exposure impedances, false colored for clarity. Electrodes are shown in descending order according to 1 kHz impedance. From left: *SiTip*, *SiSh*, *PM*, *Std*, and *NM* style electrodes. Scale bars are 300 μm. (b) EIS of all devices. Markers indicate geometric mean for impedance (left) and arithmetic mean for phase (right), taken for N = 16 electrodes per UEA. Data were taken at 10 points per decade, but one out of every three points are shown for image clarity. Shading indicates geometric and arithmetic standard deviation for magnitude and phase, respectively, which are plotted for all data points.

Table 2
Parameters from controlled material exposure measurements.

Device type	Electrode material	Mean length[a] ±SD [μm]	Est. area (bounds) [×1000 μm²]	Normalized |Z| at 1000 Hz[b] (bounds) [Ω mm²]	CPE admittance Q_0 [μS s^{-n} mm^{-2}]	CPE exponent *n*
Std	IrO_x	102 ± 7	9.9 (9.0, 11)	28 (27, 29)	27	0.87
SiTip	Silicon	92 ± 14	8.5 (6.7, 11)	9700 (9100, 10^4)	0.025	0.95
SiSh	Silicon	~1000	370	7800 (6300, 9300)	0.024	0.99
NM	IrO_x[c]	579 ± 14	120 (110, 120)	48 (48, 49)	62	0.77
PM	IrO_x[c]	84 ± 8	7.4 (6.4, 8.4)	31 (29, 33)	23	0.84

[a] Arithmetic means and standard deviations (SD) of tip lengths are reported.
[b] Geometric means and SD of impedance magnitudes were used to calculate normalized impedances.
[c] Silicon was also exposed for these devices, but only dimensions and parameters for IrO_x are shown.

estimated from mean tip lengths using the SolidWorks model described in Section 2.4, and surface area bounds were found based on mean tip lengths ± SD. Since the *SiSh* condition was a uniformly silicon UEA, no boundary delineations existed to measure and thereby derive SD values, and all electrodes were assumed to be the same overall length (1 mm) for modeling simplicity. Area-normalized impedance magnitudes were found by dividing geometric means of impedances (see Fig. 7b) by estimated surface area. We have found that geometric means represent well the distribution of impedance magnitudes measured for UEAs (Caldwell et al., 2017). For all but *SiSh-type* electrodes, impedance bounds were calculated by normalizing impedance mean ± SD (geometric) to lower and upper surface area bounds, respectively. As no surface area bounds were found for the *SiSh* condition, impedance bounds were based only on estimated area. Surface areas and normalized impedance are shown to two significant digits.

Parametric fitting of impedance data to the Randles circuit (Fig. 4 and Equation 1) was sufficient to estimate Q_0 and *n* for *Std*, *SiSh*, and *SiTip* UEAs conditions. However, the Randles circuit best represents the behavior of a single electrode material, and contributions from two distinct materials (IrO_x and silicon) were apparent in both *NM* and *PM* impedance spectra. Therefore, we employed a modified circuit of two Randles circuits in parallel in order to fit the data from these electrodes, with one circuit fitting IrO_x contributions, and the other fitting those of silicon. A summary of geometric and equivalent circuit parameters associated with each type of electrode structure is given in Table 2, which for clarity, only shows parameters for materials present at electrode tips.

3.1.1. *Std* electrodes

As seen in Fig. 7b, average impedance magnitude for the *Std* UEA was 450 kΩ at 1 Hz and decreased to 2.8 kΩ at 1000 Hz, reflecting CPE-dominant behavior typically seen for the UEA electrode interface (Caldwell et al., 2017). Phase increased from a minimum of −72° at 40 Hz to −36° at 1000 Hz as the impedance spectra transitioned from capacitive to resistive behavior. Impedance at frequencies above 1000 Hz did not decrease below 1.8 kΩ and phase approached 0°, due to the limiting effects of solution spreading resistance around the exposed tips of control electrodes (average 102 μm exposed length). This resistance is largely a function of the solution resistance and path geometry from electrode to ground, and is thus little affected by electrode surface treatments that do not alter the external environment.

3.1.2. *SiTip* electrodes

The *SiTip* condition represented a case when all electrode metal is removed and was characterized by a semi-capacitive modulus spectrum up to 1000× larger than that of the *Std* UEA, as well as a phase between −86° and −75°. This disparity between silicon and IrO_x was reflected in Q_0 parameters which also differed by three orders of magnitude, and *n* values indicated more capacitive electrode characteristics of silicon compared to IrO_x (*i.e.* *n* closer to 1). Since *Std* and *SiTip* tip exposure varied by only 10 μm, spreading resistance was expected to be similar for both devices. Such was not obvious from data shown in Fig. 7b alone, as *SiTip* impedance at the highest measured frequency was almost 10× that of the expected spreading resistance of 1–3 kΩ, based on *Std* data. However, circuit fitting of *SiTip* data did reveal a spreading resistance of 2–4 kΩ, similar to that of *Std* electrodes.

3.1.3. *SiSh* electrodes

SiSh-type electrodes completely lacked parylene C encapsulation, but *SiSh* impedance was still typically more than 10 × that of the *Std* UEA due to high intrinsic impedance of silicon compared to IrO_x, the latter being absent on *SiSh* devices. However, *SiSh* impedance did decrease below *Std* for frequencies >10^4 Hz. This was attributed to the electrolyte spreading resistance limit associated with an entire electrode shaft being 10 × lower than that of a precisely exposed electrode tip (0.2–0.4 kΩ compared to 1–3 kΩ, respectively, for devices reported here). That *SiSh* electrodes approached solution resistance at high frequencies was apparent in the phase increase from −88° at 1000 Hz to −40° at 10^5 Hz. Similarly, *NM* and *PM* devices exhibited 10^5 Hz impedances of ~0.3 kΩ and showed phase angles increasing towards or already near 0°. Since electrode shafts for *SiSh*, *NM*, and *PM* devices all lacked parylene C and were therefore fully exposed, solution spreading resistance was expected to be similar for all and this was confirmed by the data.

3.1.4. *NM* electrodes

Complete parylene C destruction to a standard UEA was represented by the *NM* case, which displayed magnitude and phase spectra similar in shape to *Std* electrodes but offset in position. *NM-type* UEA modulus was reduced an order of magnitude from *Std* modulus due to decreases in spreading resistance and electrode interface impedance, commiserate with the 10× increase in exposed IrO_x surface area. The −40° phase inflection between CPE and resistive characteristics was shifted to 250 Hz for *NM* electrodes compared to 800 Hz for the *Std* UEA, indicating that limiting solution resistance was encountered at lower frequencies for *NM* devices. This is further apparent in the perceived "flatness" of the magnitude spectrum at 1000 Hz for *NM* devices compared to *Std* and *PM*, electrodes, accompanied by *NM* phase angle being closer to 0° than those of control or *PM* devices (−20° compared to −36° and −58°, respectively). As a result, area-normalized impedance at 1000 Hz for *NM* devices was more than 60% higher than the ~30 Ω mm^2 values calculated for *Std* and *PM* electrodes. A normalized impedance of 19 Ω mm^2 for *NM* electrodes was calculated using CPE parameters and (1) in order to disregard solution resistance, indicating that spreading solution resistance increased effective *NM*-type electrode impedance at 1000 Hz by more than 150%. As an aside, it would be expected that any potential modification to the *NM* UEA in order to reduce electrode impedance would have little effect on 1000 Hz characteristics, since the solution resis-

tance limit is already reached. Although the *NM*-style electrode does not represent a fully functional neural electrode, this does emphasize how consideration of electrode geometry and spreading resistance must be taken when designing and characterization electrodes.

3.1.5. PM electrodes

The *PM*-style UEA represented complete encapsulation damage to a special case UEA, one which received tip metal length similar to *Std* tip exposure length (84 μm compared to 102 μm, respectively). *PM* electrodes displayed characteristics of both *Std* and *SiSh* electrodes, with a transition from the former to the latter occurring between 1000 and 10^4 Hz as is apparent in the magnitude and phase spectra. Exposed IrO_x was the primary contributor to *PM* impedance at 1000 Hz, which was comparable to that of the *Std* UEA. The slightly higher impedance of *PM* electrodes compared to *Std* electrodes at frequencies >1000 Hz was attributed to the reduced IrO_x surface area of the former. As previously mentioned, equivalent circuit fitting for *PM* electrodes required a parallel configuration of Randles circuits. CPE parameters fitted to the sub-circuit describing IrO_x contributions are shown in Table 2, which are also similar to *Std* parameters. Not shown in Table 2: parameters for the sub-circuit describing exposed silicon on *PM* electrodes included a Q_0 of 19 nS s^{-n} mm^{-2}, close to the 24–25 nS s^{-n} mm^{-2} range for *SiSh* and *SiTip* devices.

3.1.6. Conclusions from EIS of parametric UEAs

The similarities between *PM* and *Std* devices at frequencies of 1000 Hz and below suggest that risks of impedance reduction from dielectric damage can be mitigated, by more precisely controlling the tip metal length such that it is similar to tip exposure length. For example, an array fabricated with standard *NM*-style tip length IrO_x, but coated with parylene C and exposed per the *Std* UEA, carries the risk of 10× impedance loss across the spectrum if all the parylene C undergoes degradation (*i.e.* transition from *Std* to *NM*-style behavior). This brings with it a profoundly negative effect on the stimulation current pathway and recording characteristics. However, precise tip length which matches tip exposure confines the risk of impedance loss to frequencies >1000 Hz and restricts impedance magnitude reduction to approximately 10× at 10^5 Hz (represented by a transition from *Std* to *PM*), depending on initial electrode conditions. This relies on the high electrochemical impedance of silicon, which we found to be 200–300× larger than that of IrO_x at 1000 Hz for UEAs. The high impedance of *SiTip* electrodes even implies that dielectric defects comparable in size to tip exposure can be tolerated with no discernable effect on impedance, if such defects only expose silicon.

3.2. FEA of parametric UEA material exposure

FEA modeling was pursued to support our understanding of how material exposure (surface area) contributes to the measured impedance spectrum, and to develop a tool whereby trends could be visualized and predicted based on neural electrode architecture. In addition, knowledge gained from this tool would aid interpretation of impedance spectrum changes from material degradation *in vivo*. We first modeled the five parametric conditions of Table 1 and compared the simulation predictions to the EIS measurements. We then utilized the finite model to predict trends in impedance spectra as a function of silicon exposure, and validated this model against empirical characterization.

The IrO_x and silicon parameters for defining electrode-PBS interfacial boundary behavior (refer to (6) and (7)) were derived from values in Table 2. Silicon values were taken as the average of *SiTip* and *SiSh* parameters (Q_0 and n of 0.0247 μS s^{-n} and 0.967, respectively), while IrO_x values matched *Std* parameters. All five UEA styles were replicated utilizing identical solid models of the electrodes, with models only differentiated by a single domain partition that was positioned according to the mean tip lengths shown in Table 2. FEA results fairly accurately agreed with values and trends in the empirical measurements, despite measured differences in the material performance and real geometry across different devices (Fig. 8). Differences between measurements and models were most significant for the calculated phase at frequencies <100 Hz, with FEA results almost always reflecting increased capacitance (values closer to −90°) compared to measurements. This was expected and is due to the lack of a finite element equivalent to the charge transfer resistance R_E in our model, as we only accounted for CPE behavior at the electrode/electrolyte interface. Nevertheless, the trends found using FEA followed empirical observations, in that impedance reduction was dramatically higher with exposure of IrOx compared to Si, per unit of area.

3.2.1. Impedance as a function of Si exposure

To strengthen our understanding of how silicon influences impedance, we reconfigured our model geometry to allow for differing silicon surface area exposure while maintaining constant IrO_x surface area (Fig. 9a). This modeled insulation failure without tip metallization failure. Tip metal exposure length was held at 50 μm, which is the typical target for commercially fabricated UEAs. Impedance was calculated based on FEA material parameters already described, while varying the length of silicon exposure from 0 to 300 μm. Given the difficulty of attaining identical tip metal length and tip exposure using standard UEA manufacturing protocols, it was assumed that encapsulation damage which exposed silicon, but not tip metal, would occur a certain distance beyond the target tip exposure boundary. This would be where parylene C did not overlap IrO_x. Therefore, an insulated section 50 μm long separated the IrO_x and silicon regions.

Finite element results are given in Fig. 9b and showed overall small changes in phase and magnitude as a function of silicon exposure, including at 1000 Hz. Impedance at this frequency changed in magnitude from 3.85 to 3.78 kΩ, and in phase from −29 to −30°, across the entire silicon exposure range. These respective changes of 2% and 3% would not be typically distinguishable from measurement noise under real-life conditions. However, higher frequency impedance trends were noted from the finite element model that would be more apparent. At 40 μm silicon exposure, 10^5 Hz impedance magnitude had decreased from an initial value of 3.21–3.04 kΩ, and phase decreased from −0.6° to −10°. While a 5% change in magnitude alone would not typically constitute an observable difference for real electrodes, the change in phase provides a much more sensitive measure. From our previous empirical measurements, we had estimated that impedance effects of silicon exposure would begin to be apparent when exposed silicon and iridium oxide areas were similar. Our model results are consistent with this approximation.

To compare the different effects of materials, a 40 μm exposed region was also modeled as IrO_x (not shown) instead of silicon. All other model parameters were identical to the silicon-exposed configuration. Changing the newly exposed region from silicon to IrO_x caused 1000 Hz and 10^5 Hz magnitudes to decrease to <3.1 and <1.8 kΩ, respectively. These respective changes of 19% and 44% for IrO_x compared to 5% or less for silicon emphasize the comparatively small degree to which exposed silicon alters electrode characteristics.

3.2.2. Finite model validation

To support the accuracy of the data and trends seen in Fig. 9, we validated our model using a custom-fabricated USEA as described in Section 2.1.2. Fig. 10a shows an electron micrograph of the constructed device, while corresponding means and standard devi-

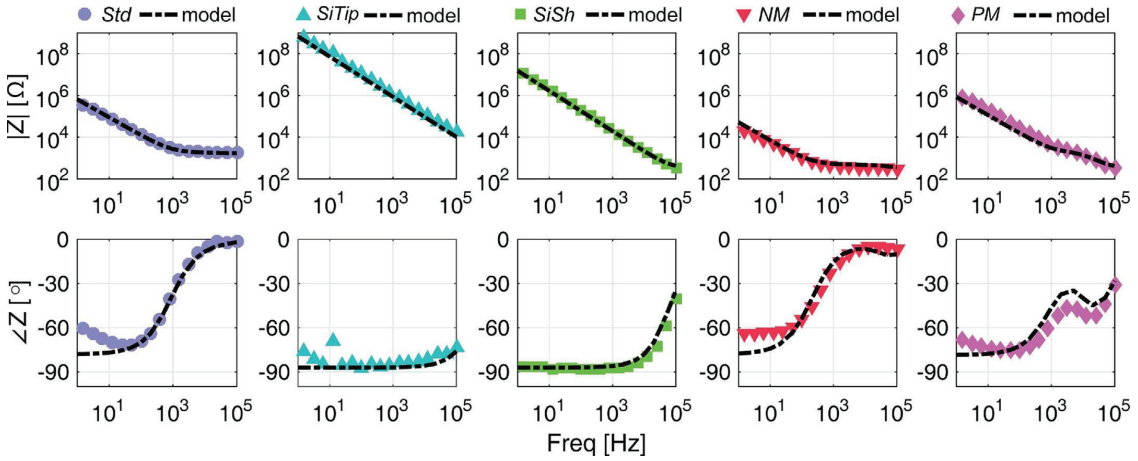

Fig. 8. FEA was performed for the five parametric conditions in Table 1 and compared to EIS measurements. Calculations are shown as dashed lines and match trends shown by corresponding empirical results (markers). Top: impedance magnitude; bottom: phase. From left: Std, SiTip, SiSh, NM, and PM devices. For clarity, standard deviations for empirical results are omitted.

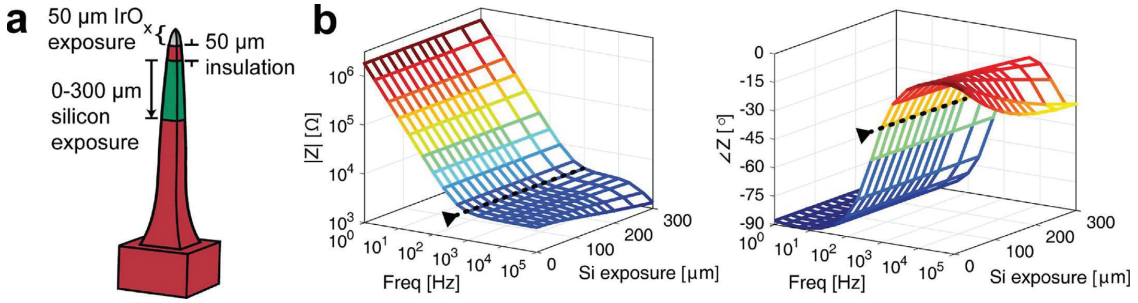

Fig. 9. FEA was conducted to find the impact of increasing silicon exposure on impedance. (a) Finite element model schematic shows constant 50 µm regions of IrO_x (gray) and insulation (red), followed by a variable length region of silicon (green). Remaining boundaries were insulated. (b) Plots of impedance (left) and phase (right) spectra show changes primarily confined to high frequencies as a function of silicon exposure length. Triangles and dotted lines mark 1000 Hz data. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

ations of electrode dimensions by row are given in Fig. 10b. Average tip metal lengths were between 42 and 67 µm, while silicon exposure varied from 22 to 280 µm. Due to differences in tip metal length, direct comparisons of 1000 Hz impedance between architectures could not be made, as differences would be primarily attributed to metal length and not silicon exposure. Therefore, we separately modeled each tip length and silicon exposure with FEA, and compared model results to empirical data. A reasonable fit between model and measurements would support that conclusions drawn from our model were sound, and Fig. 10c shows that calculations closely followed measurements for frequencies >100 Hz. At 10^5 Hz, magnitude and phase decreased with increasing silicon exposure, consistent with previous models and measurements. Silicon exposure of 22 µm did not drive obvious changes to impedance spectra compared to previously shown spectra for metallized devices with no silicon exposed (refer to *Std* data in Figs. 7b and 8). Silicon exposures of 111 µm and greater were accompanied by decreasing phase away from 0° as well as decreasing magnitude at 10^5 Hz. The presented data validated the capabilities of this finite element model to predict impedance trends based on UEA architecture.

3.2.3. FEA shortcomings

Model deficiencies did exist for frequencies <100 Hz as previously mentioned, which were most apparent for calculations of phase. These shortcomings may be addressed in future work through careful characterization of charge transfer resistance, utilizing large sample sizes and careful fabrication to ensure that characterization of this resistance is not confounded, *e.g.* by encapsulation defects. To accommodate this additional resistive element, custom equations could be implemented in the FEA environment which account for both interfacial CPE and resistive charge transfer characteristics. While such modifications might improve overall model accuracy, we did not pursue them because we only attributed nominal value to the precise modeling of sub–100 Hz impedance phase.

3.2.4. Conclusions from the finite element model

One primary conclusion from this model is that dielectric damage which exposes silicon is not likely to be detected from 1000 Hz impedance measurements. This is an important consideration when drawing conclusions regarding UEA performance *in vitro* and *in vivo*, particularly when dielectric cracking and damage is associ-

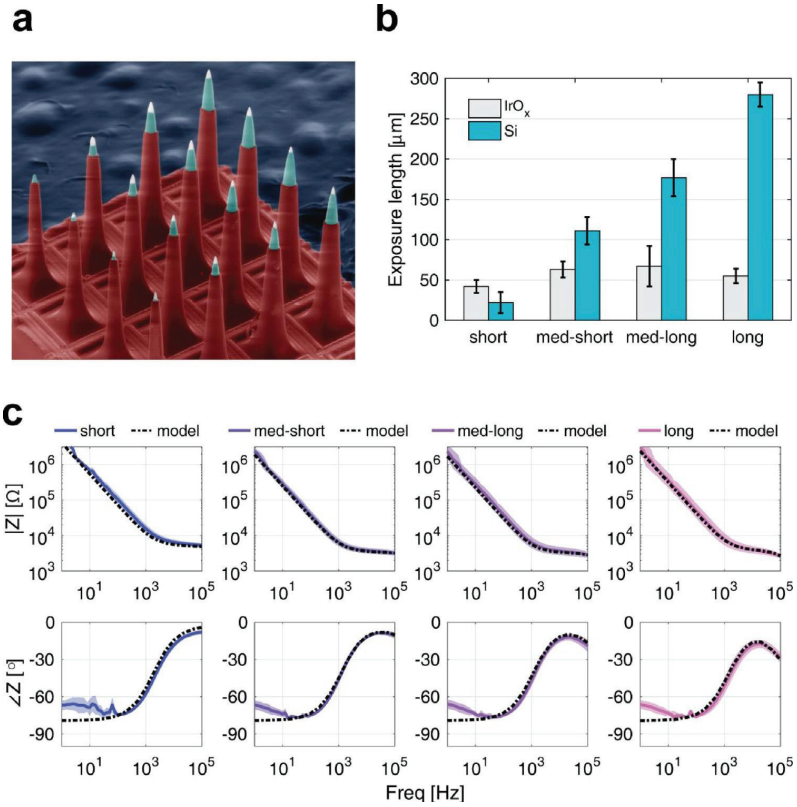

Fig. 10. FEA modeling was validated by empirical measurements. (a) False-colored SEM image of USEA used for model validation. (b) Bar plot showing mean and standard deviation of IrO_x and Si exposure on a column-by-column basis, corresponding to left-to-right columns in USEA image. N = 3 electrodes for the short row, N = 4 for all others. (c) Average and standard deviation of USEA impedance magnitude (top) and phase (bottom), on a column-by-column basis and compared to finite element calculations.

ated with poor impedance measurements and faulty performance. Observations of cracking and damage occur near the electrode tip (Barrese et al., 2016) may be justifiably associated with reduced performance, since such damage would be likely to expose tip metal and increase effective electrode surface area. Occasions in which damage is largely observed at the array base (Kane et al., 2013) must be treated with more caution, as such damage may be confined to silicon regions alone and thus would not be expected to have as strong an influence on device performance. From the data presented here, any observed drops in 1000 Hz impedance associated with the latter case would be expected to arise from other causes, such as widespread shunting between electrode bond pad sites, or unknown interactions between tissue and silicon.

A second conclusion from this model is that use of silicon as an implantable electrode conductor can bring two advantages. One clear advantage is the possibility of careful control over the degree to which impedance can change due to dielectric damage. Drawing from FEA results in Fig. 9b, an electrode design which eliminates the possibility of IrO_x surface area increasing in spite of dielectric damage (*i.e.* similar tip metal length and exposure) can almost assure unchanging 1000 Hz impedance. A byproduct of such a design, and advantage in its own right, is that it lends itself well to diagnosis of array material performance through impedance spectroscopy. Damage to dielectric encapsulation would be evident through high frequency impedance reduction, while damage to electrode metal would increase impedance magnitude, especially at low frequencies, driving the spectrum towards that of the *SiTip*-style UEA. While these trends have been repeatable for *in vitro* testing, further characterization would be needed to determine how such generalizations hold for *in vivo* applications.

Despite the advantages that silicon poses to the electrochemical performance stability of neural electrodes, it is known to slowly erode and generate non-toxic degradation products when fully exposed to the physiological environment (Low and Voelcker, 2014; Wise et al., 2004). Therefore, careful considerations must be made in electrode designs which incorporate silicon, among which is avoiding silicon exposure by design into the electrode architecture. Applied to UEAs, this requires that tip metal length be slightly larger than tip exposure to ensure the protection of underlying silicon by tip metal across the metal-dielectric transition. However, this does not negate the advantages of silicon discussed up to this point. The considerations associated with silicon etching *in vivo* are further addressed in the final section of this report.

3.3. *RAA of UEAs with 100 μm vs 300 μm tip metal length*

We tested fully fabricated UEAs with *PM*- style tip metal lengths against UEAs with *Std/NM*-style tip metal lengths in an aggressive *in vitro* RAA system (Takmakov et al., 2015) to evaluate the benefits of silicon for reducing the impact of dielectric damage on electrode performance. Four devices of N=16 electrodes each were fabricated per cohort. Experimental devices had a target tip

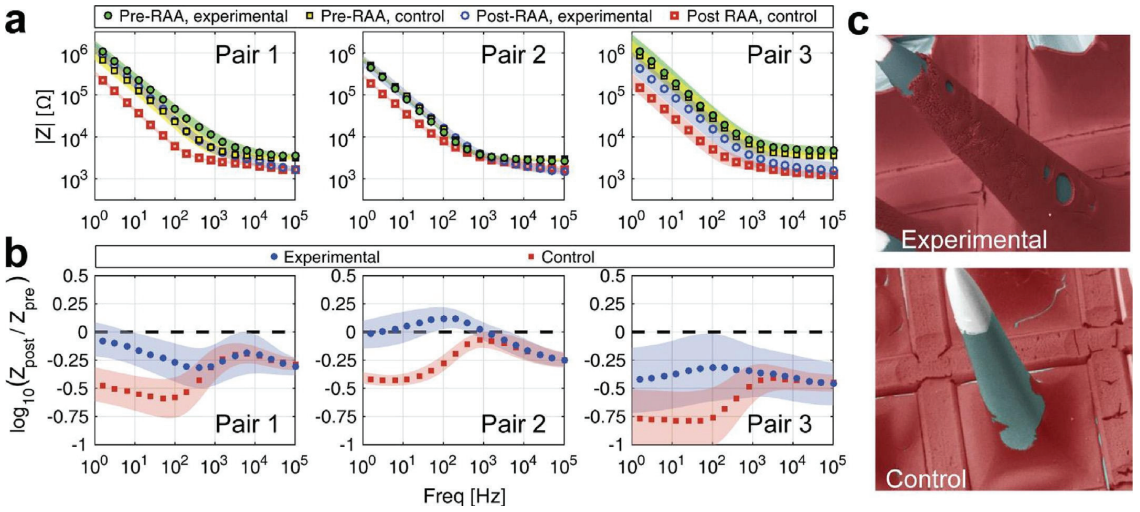

Fig. 11. RAA incurred dielectric damage and impedance change to precise and standard devices, however, the presence of precise tip metal length reduced changes. (a) Pre- and post-RAA impedance magnitude spectra grouped by experimental-control device pairs aged together, shown as geometric averages and standard deviations. (b) Average normalized change for corresponding plots in (a). (c) False colored SEM images showing examples of dielectric damage incurred through RAA testing to experimental and control electrodes.

metal length of 100 μm, actual tip length was 115 ± 22 μm. Control UEAs had a target tip metal length of approximately 300 μm, final average length was 326 ± 27 μm. Exposure lengths for all devices was targeted at 90 μm, actual lengths were 86 ± 20 μm for experimental devices and 108 ± 22 μm for controls. Devices were tested in pairs (see Fig. 3) composed of one experimental and one control UEA each, and impedance changes were noted between initial and final conditions. Handling damage during processing caused the initial impedance values for one pair of UEAs to be non-representative, hence their results are omitted from this report. Fig. 11a shows impedances measured before and after aging for the remaining three device pairs. Initial impedances were similar across all devices, exhibiting near 1000 kΩ magnitude at 1 Hz, which decreased to 7 kΩ at 1000 Hz and leveled out to 3.5 kΩ at 10^5 Hz. All devices showed impedances losses after RAA processing, with magnitudes at 10^5 Hz near 1.7 kΩ for all UEAs, a change of >50%. Post-RAA impedances for experimental and control UEAs diverged for frequencies <1000 Hz, with experimental UEAs reaching a 1 Hz magnitude of 600–1000 kΩ, and control devices having much lower 1 Hz impedance around 200 kΩ.

Normalizing final impedance magnitude to initial values (Fig. 11b) revealed that the relative changes were very similar between experimental and control devices for frequencies >1000 Hz. At frequencies <1000 Hz, experimental arrays incurred normalized impedance reductions between 0 and 0.5, while controls experienced larger normalized reductions of between 0.5 and 0.75. Computing a mean of means and standard deviation of means for these normalized values revealed the strongest effect size of 2 occurring at the 10 Hz frequency, in regards to mitigated impedance loss for experimental UEAs *versus* controls. This effect was not associated with statistical significance but was nearly so ($p = 0.06$). We expect that this effect would be detected with significance by a future study utilizing a sample size of at least N = 4 devices, as was our original intention.

From the trends and models previously discussed, low impedance magnitudes at high frequencies can be expected in cases of large surface area exposure of a conductive material, as large area reduces solution spreading resistance. This lowest-limit spreading resistance is determined solely by surface area and is independent of material coating, as is clear through the apparent convergence of *SiSh* and *NM*-style electrode impedances at high frequencies (Fig. 7b). We observed a similar degree of normalized change at high frequencies between experimental and control devices, which would be expected if all devices experienced considerable parylene C damage and commiserate shaft exposure after RAA. SEM imaging confirmed that considerable damage to parylene C during RAA did indeed occur, in some cases completely removing a majority of the coating (Fig. 11c). This has prompted further analysis of parylene C damage mechanisms for this system, and will be published in detail in a forthcoming report.

3.3.1. Comparison to prior RAA results

Previous RAA work has been performed with Michigan-style probes, floating electrode arrays, microwire arrays, as well as Pt-coated UEAs (Takmakov et al., 2015). Impedance reduction for these devices was observed to be most prominent at 1 Hz, with average normalized change ranging from −1 for microwires to −3 for UEAs. At 10^5 Hz Michigan probes showed close to no change, while remaining devices were reduced by −0.5 or more. In general, the devices tested in this report experienced impedance reduction to a much lesser degree than those previously reported, despite widespread dielectric damage. This may arise both from our modified design as well as from the comparatively low initial impedances of our devices, compared to the reported typical 1000 Hz impedance of 1000 kΩ for floating electrode arrays, Michigan probes, and Pt-coated UEAs. Notably, microwire arrays previously tested were most similar to our devices, with 2000 kΩ impedance at 1 Hz decreasing to 10 kΩ at 1000 Hz, and leveling off to 5 kΩ at 10^5 Hz. Trends for microwire impedance changes were also similar to that of our control UEAs, with most prominent reduction at frequencies <100 Hz, the least change occurring near 1000 Hz, and moderate reduction at frequencies >10^4 Hz.

3.3.2. Conclusions from RAA testing

We have been able to mitigate the low frequency changes by using precise tip length to take advantage of high intrin-

sic impedance of silicon. However, we nevertheless observed impedance reductions at high frequency. According to our results, improved impedance stability at frequencies >10^4 Hz would require: 1) a dielectric coating robust enough so as to not undergo significant degradation during use, and/or 2) a conductive shaft material with even higher electrochemical impedance than silicon.

Concerning the first point, published data suggests that in many cases the damage to parylene C *in vivo* is much more moderate than the gross damage we observed after RAA. Many studies report only parylene C cracking and localized damage (Barrese et al., 2016; Kane et al., 2013; Prasad et al., 2014; Schmidt et al., 1988), and we expect that electrode designs similar to the *PM*-style metal length tested here would greatly mitigate risks of electrode performance change in such cases. However, the dearth of literature describing profound parylene C damage *in vivo* may be due to insufficiently long implantation time points, and development of robust dielectric coatings remains a critical need. There is significant potential for the optimization of parylene for long-term implantation, and we have preliminary data suggesting its robustness can be improved under certain processing conditions. There is also ongoing work with novel electrode coatings such as silicon carbide which may further address this issue (Cogan et al., 2003; Hsu et al., 2007).

Regarding the second point, we have only begun to take notice of the unique advantages presented by electrical conductors with poor electrochemical characteristics, and conductive materials may exist that have higher electrochemical impedance than silicon. Further knowledge of how silicon characteristics contribute to electrochemical behavior may inform the development and evaluation of materials with even greater disparity between electrical and electrochemical performance. In the final portion of this report, we begin to address this last point by investigating the nature of silicon impedance as a function of silicon doping properties, compared to other common electrode materials.

3.4. EIS of silicon under various doping conditions

We characterized planar silicon electrodes with distinct doping characteristics, to advance understanding of how the silicon doping concentration and electrical properties such as Fermi energy (chemical potential) affect the electrochemical impedance. These were compared to other common neural electrode materials, which were characterized in the same manner. Electrolyte spreading resistances for all electrodes were similar and near 0.3 kΩ, indicating that electrode surface areas and measurement conditions for all materials were comparable. Area-normalized measurements of 1000 Hz impedance modulus for these materials are presented in Fig. 12. Measurements for all silicon electrode types were greater than $10^4\ \Omega\,mm^2$, while all metals and IrO_x were below $1000\ \Omega\,mm^2$. An asymptotic effect of silicon doping on impedance was observed, in that reduced resistivity of 100× and 1000× with respect to 1–20 Ω cm silicon accompanied impedance decreases of only 1.7× and 2.2×, respectively. Similar impedance values were observed for *p*-type and *n*-type silicon with similar conductance, which were chosen to detect any effects from silicon Fermi energy approaching the valence band or conduction band (for *p*-type and *n*-type, respectively). As these energy levels are at opposite ends of the silicon band gap and no impedance difference was detected, it is suggested that Fermi energy level is a poor predictor of silicon impedance compared to impurity concentration and bulk conductivity.

The highest conductivity silicon investigated here was within the range of 0.001–0.005 Ω cm. To attain 0.001 Ω cm for silicon with boron (*p*-type) and arsenic (*n*-type) dopants, the impurity concentration must be approximately $10^{20}\ cm^{-3}$. This concentration is widely taken to be the point at which charge mobility becomes saturated, and at this limit silicon is considered degenerate, in that its conductivity properties are similar to those of metal. However, in light of the >10×difference between normalized silicon and metal impedances reported here, these similarities clearly do not extend to electrochemical interactions in saline. These differences may be attributed to several reasons.

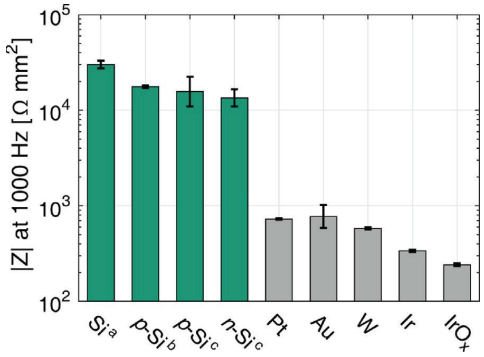

Fig. 12. Impedance magnitudes at 1 kHz for silicon substrates were found to be over 10× higher than other materials commonly used to conduct neural electrode signals along a penetrating shank. Data shown are geometric averages and standard deviations of three measurements for metals, and three to nine measurements for silicon electrodes. Superscripts indicate silicon resistivity. a: 1–20 Ω cm; b: 0.01–0.05 Ω cm; c: 0.001–0.005 Ω cm.

3.4.1. Possible explanations of high silicon impedance

One reason for high silicon impedance may arise from the nature of charge mobility within semiconductors, which is influenced by energy and concentration gradients. Semiconductor surface contact with an electrolyte solution creates a gradient at the interface between the semiconductor energy state and that of the electrolyte, resulting in redistribution of charge carriers nearest the surface until equilibrium is reached. The resulting space charge region is devoid of charge carriers due to this redistribution, and attains a capacitance characterized by the Mott-Schottky relation (Boddy, 1969; McCann and Badwal, 1982). This capacitance is small compared to that of the Helmholtz layer and the space charge region in the solution, and greatly increases the impedance of the current path from semiconductor to electrolyte.

Another factor may be the formation of surface oxides on silicone, widely known to grow in a self-limiting manner in environments exposed to oxygen and water, such as ambient air. An oxide layer may create an insulating dielectric barrier between the charged silicon surface and the double layer interface, increasing impedance. Furthermore, surface reactivity of electrolyte ions with silicon dioxide has been noted to be poor compared to other dielectrics such as aluminum oxide, resulting in higher relative electrochemical impedance for the former (Bousse and Bergveld, 1983). The nature of the Helmholtz layer may also be considerably different between metals and semiconductors due to differing ion affinities for the two material types

These explanations are simplified treatments of complex phenomena, further treatment of which is outside the scope of this study. In this work we have focused on empirically identifying the advantages of silicon use in neural electrodes and promoting a novel way to approach neural electrode design. It is interesting to note that area-normalized impedance of bare carbon fiber electrodes is comparable to that of metal electrodes reported here, despite having resistivity of 0.001 Ω cm, similar to our silicon samples (Guitchounts et al., 2013; Kozai et al., 2012; Patel et al., 2015). Thus we can be certain that the high electrochemical impedance is not due to the higher resistivity of Si compared to metals, but

to a completely different mechanism such as that just described. This also suggests that other semiconductor materials may exhibit similar characteristics.

3.4.2. Conclusions from silicon impedance characterization

Our findings suggest that a future electrode architecture designed for maximum impedance stability might be constructed using, for example, highly-doped polysilicon or silicon carbide. Such would allow for low profile conductor traces that are resilient against shunting to the electrochemical environment, while providing suitably conductive paths for electrical signals. Even though prior reports have claimed that polysilicon for neural electrodes is non-ideal owing to high resistivity (Han et al., 2012), we note that carbon fiber electrodes of conductivity similar to silicon samples reported here have been used with success (Guitchounts et al., 2013; Kozai et al., 2012). However, the different crystalline nature of polysilicon may cause it to perform differently in electrolyte solution compared to single crystal silicon, and requires performance verification.

3.4.3. Limitation of silicon as a conductor

The strategy of utilizing silicon as a current conductor is not promoted to replace protective dielectric coatings or suggested to render them redundant. Rather, it can provide an added measure of electrochemical stability against risks of small encapsulation defect formation or changes to encapsulation dielectric constant (*e.g.* through ionic fluid uptake). As previously mentioned, silicon is known to be degraded in saline (Wise et al., 2004), and we have observed clear signs of silicon etching on exposed UEA shanks after three years' implantation (to be detailed in a forthcoming report). The most detrimental effect of silicon degradation to be avoided is the undercutting of electrode films. Through undercutting, the silicon immediately underneath the electrode coating is degraded, rendering the electrode film extremely vulnerable to physical breakage. An intermetallic region exists between silicon and deposited IrO_x films of the UEA, and prior work has shown that such intermetallic regions can undergo galvanically-coupled corrosion (Ding and Hihara, 2008; Becker et al., 2010). Therefore, as we report the benefits of UEA designs which closely match tip metal length and exposure, we emphasize that tip length must be slightly longer than tip exposure to prevent direct exposure of the intermetallic region to electrolyte. Interestingly, Ding and Hihara noted that when an intermetallic region is absent, the silicon space charge region exhibits very little galvanic reactivity (Ding and Hihara, 2008), suggesting that silicon regions not immediately adjacent or underneath IrO_x metal film may be less prone to degradation. However, further work is needed to characterize silicon degradation on UEAs and other neural electrodes, and to assess what risk such degradation poses to device function.

4. Conclusion

Degradation of dielectric encapsulation on implanted neural electrodes has been noted to accompany functional failure of these devices. A hallmark of this failure mode is reduction of electrode impedance, which can result in the loss of detectable single neuronal units as well as poor neuronal response to stimulation. This has motivated us to investigate the unique electrochemical properties of highly doped silicon as a conductive neural electrode material, particularly with regard to how it may mitigate the effects of damage to dielectric encapsulation over time.

Utilizing UEA architecture as a basis for our characterization efforts, we investigated the contributions to the impedance from all materials used to fabricate UEA electrodes as a function of surface area. This was to better understand the implications of encapsulation degradation, develop architectures with increased resilience to degradation, and develop models and frameworks to assess electrode degradation by measuring impedance spectra. The area normalized electrochemical impedance of silicon was found to be on the order of $10^4\ \Omega\,mm^2$ at 1000 Hz, more than 100× that of the IrO_x electrode film deposited on UEA electrode tips. This high impedance resulted in negligible effects of exposed silicon on electrode characteristics, as compared to identical IrO_x exposure. We developed and validated a finite element model that supported our characterization efforts, and found that precise electrode design utilizing conductive silicon shanks can render 1000 Hz impedance characteristics more resilient to changes from dielectric damage. This is accomplished by fabricating electrodes such that dielectric damage is most likely to only create shunting paths through conductive silicon. Reactive accelerated aging of UEAs confirmed that precise electrode architectures incorporating silicon conductive elements undergo reduced impedance change (effect size of up to 2) in aggressive environments compared to standard UEA designs. We found an asymptotic effect of silicon doping on impedance, with >1000× increase in doping concentration and commiserate decrease in resistivity from ~1 to ~0.001 Ω cm accompanied by electrochemical impedance reduction of only 2.2×, at 1000 Hz. Furthermore, at the lowest investigated resistivity of 0.001–0.005 Ω cm, silicon impedance remained >10× higher than that of common neural electrode materials, as well as that of impedances reported for carbon fiber electrodes of ~0.001 Ω cm resistivity.

We conclude that silicon has several benefits when used in the construction of neural electrodes, including suitable bulk conductivity, diverse microfabrication techniques, and high electrochemical impedance that inhibits the formation of external shunt paths. However, a clear drawback exists in that it is gradually eroded if fully exposed to the *in vivo* environment, a moderate risk to electrode performance that can be mitigated through careful electrode design. This work will help inform future electrode architectures to drive electrode technology towards more stable long-term performance and clinical applicability.

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CHAPTER 4

ELECTRON MICROSCOPY AND SPECTROSCOPIC CHARACTERIZATION OF AGED NEURAL MICROELECTRODES: COMPARING DIELECTRIC MATERIAL DEGRADATION *IN VIVO* TO REACTIVE ACCELERATED AGING

4.1 Abstract

As integral components of neuroprosthetic technologies, implantable neural microelectrodes can transform treatments for limb loss, paralysis, and other neural disorders. However, dielectric material degradation during chronic indwelling periods restricts device functional lifetimes to a few years, and has significant variability, which impedes clinical viability. To better understand the factors contributing to material degradation and inform the design of tests capable of simulating *in vivo* failure modes, we characterize parylene C-coated Utah electrode arrays (UEAs) using electron microscopy, as well as absorption and emission spectroscopy. Arrays implanted in feline peripheral nerve for 3.25 years were explanted and compared to devices aged using reactive accelerated aging (RAA), a soaking bath comprised of phosphate buffered saline (PBS) + 20 mM H_2O_2 at both 67 or 87 °C (soak times of 28 and 7 days, respectively). Similar physical damage characteristics were noted between explanted devices and arrays aged using RAA at 87 °C, and parylene C degradation was overwhelmingly apparent for

UEAs from both RAA cohorts, while being all but absent for control devices aged in PBS alone. Spectroscopic characterization found clear indications of oxidation and chlorine abstraction for parylene C aged *in vivo*, and while *in vitro* aging was also accompanied by signs of oxidation, *in vivo* and *in vitro* measures were significantly different. Analysis of RAA-aged devices identified UEA fabrication approaches that may greatly improve device resistance to degradation. This work highlights the value of spectroscopic modalities and RAA in identifying material and device failure modes, and the ongoing need to better understand *in vivo* damage mechanisms to better inform device testing and design solutions.

4.2 Introduction

The performance of medical devices is intrinsically linked to the performance of materials used in their construction, with material degradation resulting in device failure. A review of medical device recalls by the FDA during 2013 and 2014 revealed materials to be a major or possible cause in over 30% of instances [1], [2]. Ideally, such outcomes are avoided through robust material testing to identify material choices appropriate for each application. We are concerned with the material performance of neural microelectrodes, which have the potential to improve the lives of millions living with disabilities such as limb loss, spinal cord injury, and motor deficits [3]–[6]. The development of robust electrode technologies is an active research pursuit, as implantable neural microelectrodes have yet to reliably demonstrate continuous functionality for 10 years or more *in vivo*, the accepted metric for clinical viability [7]. Meeting this metric will require improved designs informed by rigorous testing of architectures and materials.

For implantable devices in general, such testing occurs both on the bench top/*in vitro*, and in animal models. All material tests include analyses of biocompatibility per ISO 10993, based on the nature and duration of material contact with physiology. Additional tests evaluate device sterility, shelf-life, shipping, and implantation lifetime. Lifetime tests can involve mechanical or electrical loads relevant to device operation [8]–[11], and commonly include exposure to an aqueous environment that approximates ionic physiological fluid and tissue, such as phosphate buffered saline (PBS).

In vitro testing timeframes are often shorter than device lifetimes, necessitating test strategies that can predict lifetimes or accelerate device aging based on expected physiological exposure. One of the most common *in vitro* testing paradigms is soak testing in PBS or similar saline solutions, at 37°C or above to represent exposure *in vivo* in real-time or accelerated aging, respectively [12]. This testing serves to evaluate water ingress, dissolution/hydrolysis reactions, corrosion, hydration/swelling, and changes in material properties that occur in the *in vivo* environment. Such tests have been a useful first step in determining material robustness, particularly of protective barrier films and packaging strategies. The material performance of neural microelectrodes has been commonly assessed in this manner [13]–[19]. Through impedance measurements, the lifetime of encapsulation strategies against fluid ingress and degradation can be assessed to test improved encapsulation materials and processes, and inform better neural electrode design.

However, *in vitro* saline testing does not represent important degradation mechanisms present *in vivo* . This results in *in vitro* testing significantly underrepresenting important degradation mechanisms observed from long-term implants,

giving rise to unexpected outcomes and poor projection of device useability. For example, Hämmerle *et al.* found that a thermally grown silicon dioxide dielectric layer that remained unchanged after 21 months *in vitro* nevertheless completely etched away *in vivo* after 10 months, leading to failure of an implanted photodiode retinal prosthetic [16]. Polyimide-insulated tungsten microwire arrays are known to degrade *in vivo* [20], but this degradation is not predicted by aging in physiological saline alone [21]. We are interested in the performance of parylene C (PPX-C), highly regarded for medical device applications due to its conformal deposition, low dielectric and moisture permeation properties, and USP Class VI classification [15], [19], [22]–[26]. Numerous reports of testing PPX-C lifetime *in vitro* [18], [23], [27] have failed to replicate the damage mechanisms reported from *in vivo* studies that have been associated with loss of performance or device failure, including cracking, delamination, erosion, and cratering [28]–[31]. The underlying causes of such degradation have not been elucidated, and novel *in vitro* test beds that reproduce this damage may not only offer clues concerning the mechanisms, but also a rapid manner for evaluating potential solutions.

A modification to the typical *in vitro* soaking paradigm that may better mimic one aspect of *in vivo* aging is the addition of oxidative species to the saline testing solution. Oxidation species are known to be generated by microglia, macrophages, and neutrophils activated as part of the foreign body response[32]. These cells release reactive oxygen species (ROS) such as hydrogen peroxide (H_2O_2), superoxide anion ($\bullet O_2^-$), and hydroxyl radical (•OH). Signs of oxidative stress have been observed to persist at neural implant sites for >8-16 weeks [33], [34], and long-term exposure to such conditions may degrade microelectrode materials. *In vitro* studies incorporating H_2O_2, the most readily replicated

and controlled ROS [35], have noted accelerated tungsten microwire electrode corrosion [21], [35], similar to corrosion observed *in vivo* [20]. Parylene polymers undergo thermal and photolytic oxidation [36], [37], and parylene damage from thermal oxidation has been proposed to occur via methylene-ester transformation and chain scission [38]. Oxidation-induced ester groups in PPX-C would be vulnerable to hydrolysis *in vivo* [39]–[41], and may be a mechanism that contributes to PPX-C damage. A closer evaluation of oxidation effects from PPX-C aging is warranted.

Takmakov et al. have published on an oxidative reactive accelerated aging system (RAA) for accelerated aging of neural microelectrodes, by soaking in an 87°C bath composed of PBS with 20 mM H_2O_2. Four types of devices were aged, including Utah Electrode Arrays (UEAs) and microwire arrays [21], which used PPX-C and polyimide encapsulation, respectively. While impedance losses were observed for all four microelectrode types tested, as well as damage to polyimide, little physical PPX-C degradation was initially observed by electron microscopy, contrasting with prior reports of *in vivo* PPX-C damage [21]. However, through additional RAA testing and detailed characterization of larger sample sizes, we have found that PPX-C does indeed repeatably occur, and exhibits similarities to *in vivo* degradation. Furthermore, we possess a previously unpublished dataset comprised of two Utah slanted electrode arrays (USEAs) explanted after 3.25 years' dwell time in feline femoral and sciatic nerve [42], which exhibit PPX-C damage characteristics similar to those of previous reports. Through characterization of these devices and comparison to RAA-processed UEAs, we aim to elucidate causes of *in vivo* degradation, and determine how well RAA models the impact of chronic implantation on medical device materials.

A key component of our study is the use of material characterization techniques to probe damaged PPX-C film chemistry and inform potential solutions. To date, most characterization efforts for neural electrodes have been limited to electron microscopy and electrochemical measurements, *e.g.* impedance (for example, see [20], [21], [28], [31], [43], [44]). However, these modalities provide limited information regarding chemical changes to materials that may drive degradation. Additional emission and absorption spectroscopic techniques can be used to probe film chemistry, but have not been used on neural microelectrode thin films owing to the difficulty of sample preparation [19]. In the first known attempt to characterize neural microelectrodes to such a degree, we employ new preparation methods to enable spectroscopic analysis such as energy dispersive X-ray spectroscopy (EDS), X-ray photoelectron spectroscopy (XPS), and Fourier transform infrared spectroscopy (FTIR) of PPX-C films on UEAs and USEAs. Our results suggest that film oxidation occurs *in vivo*, and that *in vivo* and *in vitro* film damage may be influenced by device fabrication protocols that can facilitate oxidation. This work enhances the understanding of the physical degradation that has been reported in previous studies, and will help inform future design and testing of neural microelectrodes and other implantables to improve long-term performance reliability.

4.3 Materials and methods

Devices characterized in this study included 2 USEAs explanted after 3.25 years in feline peripheral nerve, as well as 20 UEAs aged using the RAA-protocol, with an additional 8 control UEAs aged in PBS (without H_2O_2). Since USEAs were part of a separate study into functional nerve stimulation [42], pre-implant characterization data

are limited. All UEAs were characterized before *in vitro* aging using scanning electron microscopy (SEM) and electrochemical impedance spectroscopy (EIS). All USEAs and UEAs were characterized post-aging using SEM, EIS, and using absorption and emission spectroscopic techniques. PPX-C-coated test structures (13 total) were included in each RAA and control run to further aid our understanding of encapsulation degradation. To comprehensively characterize the degradation mechanisms, 7 different types of reference samples were required, primarily to facilitate our understanding of spectroscopic results and account for possible effects of sample preparation. Figure 4.1 shows an illustration of a UEA, as well as the novel sample preparation techniques that were developed.

4.3.1 UEA fabrication and PPX-C encapsulation

UEA construction has been reported at length [45], [46] and proceeded from *p*-type boron-doped silicon (0.01-0.05 Ω cm, Virginia Semiconductor, Fredericksburg, VA), which was diced, processed, and etched to create 4×4 arrays of sharp silicon tines 1 or 1.5 mm in length, electrically isolated by glass-filled kerfs. Iridium oxide was deposited on tips of the silicon tines by reactive sputter deposition [47], [48]. Platinum was sputter deposited and lithographically patterned on the planar UEA backside to create wire bond pads.

After metal deposition, devices were encapsulated with PPX-C. The encapsulation process began with 2 hours' exposure to vapor-phase A-174 silane adhesion promoter (Momentive Performance Materials, Waterford, NY). PPX-C films of 5-6 µm thickness were then deposited from DPX-C dimer in a PDS 2010 (both from Specialty Coating Systems, Indianapolis, IN). Film thickness was verified on witness

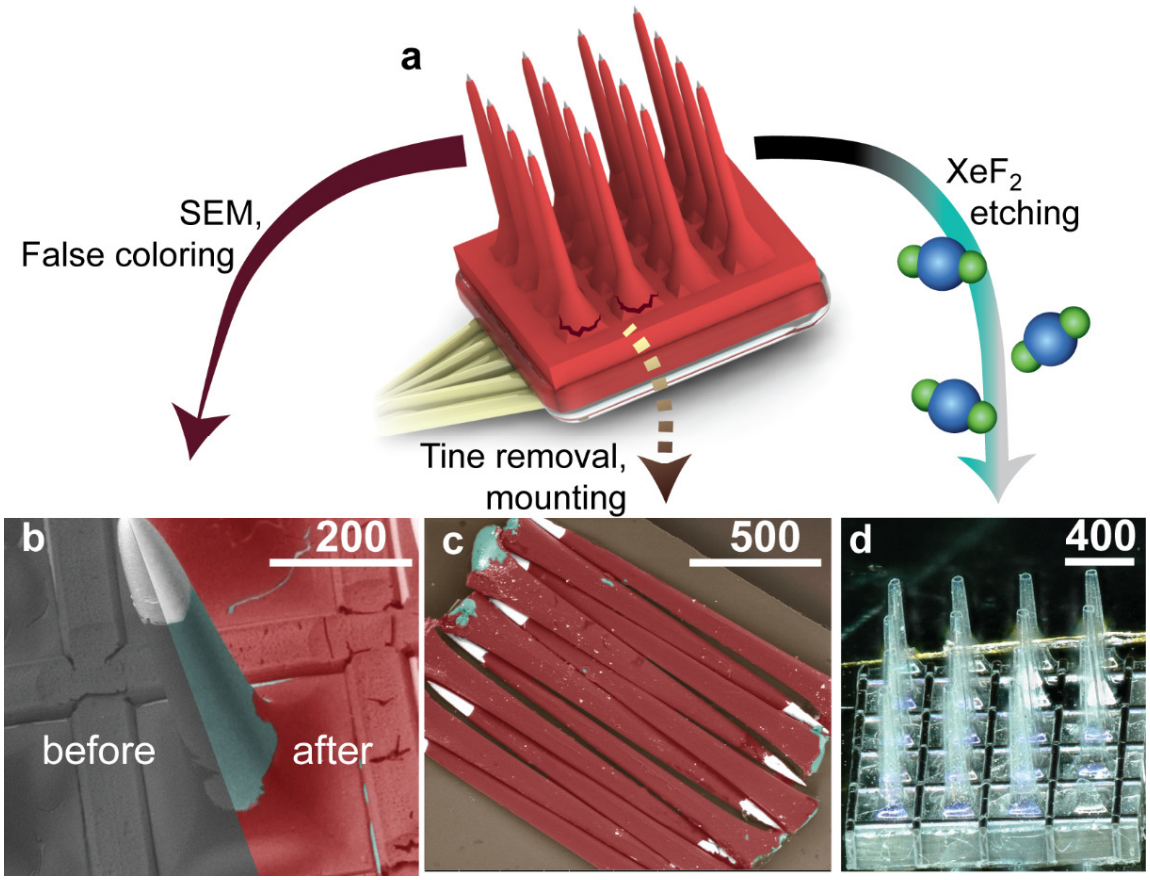

Figure 4.1 Illustrations and micrographs of UEAs and sample processing employed in this report. (a) Diagram of UEA, highlighting processing techniques shown in (b)-(d). (b) Micrograph of an electrode tine shows how raw images ("before") were false colored ("after") to enhance contrast between materials. All false coloring delineates iridium oxide (white), silicon (blue-green), and PPX-C (red). (c) Electrode tines were removed from the UEA body and laid tip-to-base to form a pseudo-planar surface for XPS characterization. (d) Optical micrograph shows a UEA after silicon removal via XeF_2 etching, leaving hollow PPX-C sheaths that were removed and place on adhesive in a similar configuration to (c) for FTIR analysis.

substrates by scoring the film with a sharp blade and measuring step height with a profilometer (Tencor, Milpitas, CA). Adhesion tests were performed on silicon monitor wafer pieces using the ASTM D3359 protocol (tape test), and acceptable scores of 4B-5B [49] were found for all deposition runs.

UEA electrode tips were exposed by etching PPX-C using an oxygen plasma deinsulation process. The UEAs were packaged in a second aluminum foil mask such that 50-100 µm of the tips penetrated through the foil, and etched in O_2 plasma (March Plasma Systems, Inc., Concord, CA) until the exposed PPX-C was removed. The etch durations were typically 18-24 minutes at 100 W and 0.4 Torr, and parylene removal was easily verified through backscatter electron microscopy (BSEM) owing to the high Z-contrast between iridium oxide and parylene.

After deinsulation, UEAs were manually wire bonded (West Bond, Anaheim, CA) to gold-flashed printed circuit boards (Circuit Graphics, Salt Lake City, UT) using polyester enamel-insulated gold bonding wire (99% Au:1% Pd) (Sandvik, Stockholm, SWE). Bond pads and wire were overmolded with MED-4211 silicone (NuSil, Carpenteria, CA) for electrical insulation and physical reinforcement.

4.3.2 Test structure fabrication

The purpose of test structures was to permit additional characterization of film damage from *in vitro* processing, in a manner complementary to UEA characterization. Two types of structures were used: interdigitated electrodes (IDEs, N=4 total) and test arrays (t-UEAs, N=9 total). IDEs were fabricated from fused silica wafers (Hoya, Tokyo, JPN) and encapsulated with PPX-C, as previously described [18], [27], [50]. The planar

nature of IDE test structures offered more minimally processed test structures and facilitated spectroscopic characterization with minimal sample preparation, and ability to sensitively measure changes in encapsulation impedance. The t-UEAs were fabricated from un-metallized UEAs, which were mounted to insulated copper wire using silicone and completely encapsulated with PPX-C. Specifically, the tips of t-UEAs were not exposed through PPX-C through oxygen plasma processing. Therefore, t-UEAs differed from UEAs in that they were not subject to metal deposition, oxygen plasma, or wire bonding. Comparison of PPX-C aging on t-UEAs with that of fully fabricated UEAs enabled detection of manufacturing-induced effects, particularly the impact of oxygen plasma processing. IDEs were not ideal for this purpose as they lacked UEA topography, which we have shown to be an important factor to consider when evaluating encapsulation performance [18].

4.3.3 Reactive accelerated aging (RAA)

RAA aging was performed in a jacketed flask (Pine Research Instrumentation, Durham, NC) filled with 20 mM H_2O_2 in PBS, prepared using deionized water and prefabricated PBS tablets (Sigma Aldrich, St. Louis, MO). The solution temperature was controlled using a Haake C-25 recirculating heater with mineral oil (Fisher Scientific, Pittsburgh, PA). Thermostat set points were set slightly above target to achieve flask conditions that did not vary more than 1 °C from desired temperatures, verified with a glass thermometer. RAA temperatures of 67°C and 87°C were employed, based on respective nominal PBS soak testing (non-RAA) aging acceleration factors *f* of 8× and 32× at those temperatures [18], [27], [50], compared to physiological conditions. These

acceleration factors are derived from empirical Arrhenius modeling of accelerated reactions according to (1.1) [12]. The temperature of 87° was chosen as the highest acceptable accelerating aging temperature, based on prior work [21]. Aging at 67 °C was also performed to begin investigating the underlying reaction kinetics for the degradation of PPX-C, and to make a preliminary determination if additional failure modes are activated by the use of temperatures that might exceed the glass transition temperature (T_g) of PPX-C. Note that the aging kinetics depend much more on the polymer due to differences in the chemistry of oxidation. Additionally, extensive aging of both UEAs and IDEs in PBS at 67 °C has been previously reported and provided a dataset for comparison to the results of this study [18]. Table 4.1 gives a summary of the experimental design and sample sizes employed in this work.

Strategies for maintaining H_2O_2 concentration varied by temperature. The half-life of H_2O_2 at 87 °C was known from previous work to be 20-30 minutes, and pumps were appropriately configured based on established protocols to keep H_2O_2 concentration at 15-20 mM, by delivering concentrated H_2O_2 and removing excess solution at fixed intervals. Flask concentration was monitored using offline UV-Vis spectroscopy at 240 nm (Ocean Optics, Dunedin, FL). Manual adjustments to pump timing were made based on daily measurements and comparisons to a 20 mM H_2O_2 reference cell, and H_2O_2 concentration in the RAA flask throughout testing at 87 °C was maintained to within 25% of the target. To reduce supervision for the lengthier 67 °C run, the RAA system was upgraded to maintain H_2O_2 concentration via closed-loop control. For this case, solution was sampled every 6 minutes by an inline UV-Vis detector measuring absorbance at 250 nm (REACH Devices, Boulder, CO), and used for closed-loop control

Table 4.1

Summary of RAA experimental design.

Aging condition	Duration (days)	Sample number (N)		
		UEA	IDE	t-UEA
RAA, 87°C	7	14	4	3
Control (PBS), 87°C	7	6		3
RAA, 67°C	28	6		3
Control (PBS), 67°C	28	2[a]	[a]	[a]

[a]Considerable testing of identical devices under the specified condition has been presented in prior publications [18], [27], and was considered in our analysis of the present work to avoid experimental repetition.

the of the H_2O_2 at 15 mM. This control strategy maintained the concentration within less than 10% of the target. Being a significant improvement to the previously reported system, it will be described in detail in a forthcoming publication.

The arrays and test structures were attached to custom-machined 24/40 PTFE flask stoppers (refer to Figure 3.3) using silicone to allow their placement in the RAA solution and prevent evaporation, with up to four stoppers and their associated samples placed in the RAA system simultaneously. To determine the effects of H_2O_2 compared to traditional saline soak testing, and confirm the higher 87 °C aging temperature did not activate additional failure mechanism through exceeding the glass transition temperature (T_g, 35-150°C [51]–[53]) of the PPX-C, control devices were aged in PBS alone at 87°C and 67°C for minimum durations of 7 and 28 days, respectively. Details on control sample sizes and conditions are presented in Table 4.1.

4.3.4 USEA explant details

The explanted USEAs described in this study were used to record and stimulate motor and sensory neural activity, which has been reported. Details regarding the objective, surgical procedures, and experimental protocols for the implants are reported elsewhere [42]. Briefly, three 10×10 USEAs were fabricated with IrO_x tip metal and PPX-C of 2.8 µm nominal thickness. They were sterilized in ethylene oxide (EtO) at University of Utah hospital, and implanted in the left sciatic and femoral nerves of an adult feline female under protocols approved by the University of Utah Institutional Animal Care and Use Committee. After 3.25 years, the feline was euthanized with intravenous saturated KCl and two arrays were carefully extracted from unfixed tissue. To remove tissue residue, USEAs were soaked overnight in ENZOL® enzymatic detergent prepared according to manufacturers' instructions (Johnson & Johnson, New Brunswick, NJ), followed by a gentle rinse in deionized water.

4.3.5 Electrochemical impedance spectroscopy (EIS)

UEAs were electrochemically characterized via two-electrode EIS utilizing a large platinum wire (>24 mm^2) as both counter and reference. Measurements were conducted with a Reference 600 potentiostat (Gamry Instruments, Warminster, PA) from 1-10^5 Hz at 10 points per decade, utilizing a 25 mV RMS excitation signal. PBS for electrochemical measurements was prepared with 140 mM NaCl, 2.6 mM KCl, 1.8 mM KH_2PO_4, and 10 mM Na_2HPO_4. Arrays were measured either in PBS alone, or a PBS-agar hydrogel. The hydrogel was prepared by mixing PBS with 2-hydroxyethyl agarose (Sigma Aldrich, St. Louis, MO) at 150 °C, and allowing the mixture to cool and form a

gel. EIS conducted using hydrogel and PBS alone verified that no differences in measured electrical properties for devices resulted from the different media.

4.3.6 Electron microscopy and focused ion beam milling

All USEAs, UEAs, and most test structures were imaged with a Quanta 600 FEG using secondary electron and backscatter electron detectors in low vacuum mode (FEI, Hillsboro, OR). Chamber water pressure of 0.15 Torr, and a 15 kV primary beam energy prevented charging while eliminating the need for sample preparation techniques such as gold coating. Secondary electron imaging helped to distinguish surface topography, and backscatter imaging distinguished materials through atomic number (Z) contrast.

High-resolution imaging and cross sectioning for PPX-C thickness measurements were performed utilizing a Helios NanoLab 650 (Thermo) equipped with a magnetic immersion lens, secondary electron detector, and gallium focused ion beam (FIB) column. Samples analyzed in this way included USEA explants and two UEAs aged with RAA at 87 °C. To prevent charging and drifting during ion beam milling for cross-sectional views, arrays were carefully stripped of silicone and wires, and platinum wire bond pads were mounted against conductive carbon adhesive. Gaps between carbon adhesive and bond pads were filled with colloidal carbon. Immersion imaging parameters were a 2 kV primary beam energy, and 50 pA current. Prior to ion milling, a thin platinum strap was selectively deposited over the viewing region to further reduce charging and image drift, and ~1 µm thick platinum strap was created over the cross section location to protect local surface topography. Milling occurred at 30 kV primary beam energy for the Ga source, and current varied from 80 pA for fine cross section

cleaning, to 2.1 nA for rapid large area removal.

To facilitate explanation and interpretation, micrographs in this report were enhanced in Photoshop (Adobe, San Jose, CA) to more clearly convey material differences. Materials were identified in raw greyscale images by combining information from secondary electron and backscatter micrographs, on-site spectroscopic measurements (*e.g.* EDX analysis), and extensive experience with and knowledge of UEA imaging and the associated contrast mechanisms. Delineations between iridium oxide, silicon, PPX-C, silicone, and other materials were highlighted with a consistent false color scheme, as shown in Figure 4.1(b).

4.3.7 Energy dispersive X-ray spectroscopy (EDS)

EDS is a semi-quantitative technique to measure sample composition, and was performed with a liquid nitrogen-cooled lithium-drifted silicon detector (EDAX Inc., Mawah, NJ) integrated into the Quanta 600 FEG. Samples were analyzed without further preparation. Standardless spectra over 60×60 μm^2 areas of PPX-C were collected for 50 seconds using a beam accelerating voltage of 20 kV and spot size of 4, at 3000× magnification. This generally yielded counts per second greater than 3000, processing dead times over 20%, and a probe depth that exceeded PPX-C thickness. Oxygen and chlorine atomic percent (at%) were normalized to carbon at% and analyzed for trends.

4.3.8 X-ray photoelectron spectroscopy (XPS)

XPS complemented EDS elemental composition data as well as provided insights into chemical bonding. To attain sufficient signal from UEA measurements, a sample

preparation techniques was developed to approximated planar surfaces (Figure 4.1(c)). This increased the area fraction of the sample in the analysis area, defined by the region illuminated by the primary X-ray source, allowing excited photoelectrons to enter the energy analyzer. Using a silicon dicing blade (DISCO Corporation, Tokyo, JPN), electrode tines were manually scored near the array base and broken off using tweezers. They were then laid side by side on high vacuum-rated adhesive, in an alternating tip-base pattern that minimized adhesive exposure between shanks. XPS was performed over sample centers to maximize signal from parylene-coated regions. As the employed adhesives contained oxygen complexes, care was taken in preparation of samples, controls, and references, as well as in data analysis, to prevent oxygen artifacts from adhesives and misinterpretation of aged PPX-C chemistry. Electrodes were only used in sample preparation if they exhibited >50% PPX-C coverage.

XPS spectra were collected with AXIS Ultra DLD system (Kratos Analytical, Manchester, UK). Samples were pumped overnight to ~10^{-8} Torr prior to being introduced to the ultra-high-vacuum analytical chamber. As XPS is a surface-sensitive technique, argon beam sputtering for 0 (as received), 30, and 180 seconds prior to spectra collection permitted depth profile measurements. Spectra were collected using a monochromatic Al Kα source (1486.7 eV). Low-resolution survey scans were collected at a pass energy of 160 eV and 1 eV step size while high-resolution region scans were collected at 40 eV pass energy and 0.1 eV step size. To mitigate the effect of surface charging, samples were flooded with low-energy electrons from the built in charge neutralizer, with the operating parameters optimized to produce a narrow O 1s and C 1s photoelectron peak. Collected spectra were analyzed and deconvoluted using CasaXPS

software. High-resolution photoelectron peaks were corrected for binding energy shift by referencing the C 1s peak of aliphatic C at 284.5 eV [54]. Deconvolution of C to O bindings in the C envelop was performed by first quantifying C to Cl percent using the Cl envelope. This was assigned to the C envelope along with fitted aliphatic C peak, and the residual envelope area was fitted to approximations of C to O binding peaks, as well as aromatic C satellite peaks.

4.3.9 Fourier transform infrared spectroscopy (FTIR)

Attenuated total reflectance (ATR) FTIR complemented XPS characterization of chemical bonds, in particular regarding the detection of carbon-oxygen complexes. This approach required clamping PPX-C flush against the ATR crystal, which was impossible if the parylene remained on UEA electrodes. To selectively remove silicon while preserving PPX-C film, samples were subject to dry isotropic XeF_2 etching in a Xetch system (Xactix Inc., Pittsburgh, PA), at 3 Torr XeF_2, and 4 torr N_2, with 18 sec dwell time and a minimum of 200 etch cycles. This preparation was destructive (Figure 4.1(d)) and created C─F complexes that interfered with XPS measurement of carbon oxidation. Therefore, all other characterization preceded FTIR. PPX-C was stripped from etched arrays and laid on vacuum grade adhesive to form a blanket. Silicone-based adhesive was used due to its flat absorbance spectra between 1500 and 2000 cm^{-1}. As ATR-FTIR probe depth of ~2 µm at 1000 cm^{-1} could exceed the thickness of damaged parylene, use of silicone adhesive ensured the integrity of carbonyl peaks near 1700 cm^{-1}.

PPX-C absorbance was measured with a Nicolet 6700 (Thermo Fisher Scientific, Waltham, MA) equipped with a single bounce diamond Smart iTR accessory, a

deuterated triglycine sulfate detector, and a KBr/Ge beamsplitter. Spectra were taken from 650 to 4000 cm^{-1} at 4 cm^{-1} resolution, averaged over 256 scans, and corrected for ATR spectral aberrations utilizing included functionality within OMNIC software (Thermo). Spectra were area-normalized to the C═C─C stretch peak near 1606 cm^{-1}.

4.3.10 Reference samples for spectral characterization

Reference samples were used to control for and validate sample preparation methods, and aid interpretation of spectral results concerning the chemical nature of PPX-C damage. Samples typically consisted of PPX-C deposited on polished silicon or UEA substrates, according to the PPX-C deposition process already described. Additional processing is outlined in Table 4.2, along with the intended case each sample was meant to reference.

4.3.11 Statistical processing

Post-hoc statistical tests were performed on data to quantify trends in the data, and support or refute the associated hypothesis. The sample size of UEAs explanted after long indwelling periods was particularly limited, therefore statistical tests were not used to draw conclusions regarding the general nature of *in vivo* aging compared to RAA or other conditions. Rather, tests were only performed to strengthen our understanding of the data presented here, to inform future studies and development as well as drive improved study and test design. Analysis was performed using IBM SPSS Statistics version 24 (IBM, North Castle, NY). Groups selected for analysis were tested for significance with Welch's ANOVA to account for unbalanced sample groups, as well as unequal variance,

Table 4.2

Reference samples employed for EDS, XPS, and FTIR spectroscopic characterization.

Description	Reference case	Postprocessing of PPX-C
Planar, untreated	•Pristine	•None
Planar, thermally oxidized	•Oxidation, aliphatic break damage [38]	•55 minutes at 250 °C in air
Planar, O_2 plasma etched	•Direct plasma exposure, aromatic ring damage [55]	•4 minutes' plasma etch (film not fully etched)
Planar, EtO sterilized	•EtO effects on pristine case, for comparison to explant spectra	•EtO sterilization at University of Utah Hospital
Planar, EtO + ENZOL	•EtO + ENZOL effects, for comparison to explant spectra	•EtO sterilization followed by ENZOL cleaning process
UEA[a], not deinsulated	•Pristine film on UEA	•None
UEA[a], deinsulated	•Plasma processing effects on remaining (on-shaft) PPX-C	•Complete plasma etching of PPX-C on electrode tips

[a]UEA references that were characterized with FTIR were by necessity subject to XeF_2 etching beforehand.

determined through Levene's test. Games-Howell post-hoc tests were done to compare group means. A value of p=0.05 was considered significant.

4.4 Results

Strong similarities were observed via SEM between *in vivo* and 87 °C RAA UEAs, and chemical analyses revealed changes between unaged and aged (including *in vivo*, PBS, and RAA) samples. Since the ideal accelerated aging test system will mimic material damage mechanisms observed *in vivo*, explant results are considered a benchmark against which *in vitro* accelerated aging methods are compared. We regarded aging process controls as representative of the current prevailing bench top aging techniques which utilize only temperature-controlled PBS or similar electrolyte. RAA results showed how modifying such existing test methods to include oxidative chemistry drives outcomes towards *in vivo* results. As changes to PPX-C condition were the primary focus of this work, post-aging electrode metal and silicon structure are only described in brief.

4.4.1 Electron microscopy

Electron microscopy permitted visualization of morphological changes and damage to electrode materials, and compositional analysis via EDX. Clear changes seen for *in vivo* and RAA (67 and 87 °C) UEAs compared to the pre-aging state and PBS controls. In general, damage to arrays as observed through electron microscopy was consistent between electrodes within each array. Therefore, images of electrodes are representative of the arrays from which they originate. Differences are seen between

electrode shapes for *in vivo* devices, due to the nonuniform electrode lengths of USEA architecture. Short electrodes for these devices tended to be blunter than long electrodes, as is apparent in the images of short electrodes on the femoral array (Figure 4.2) compared to longer electrodes on the sciatic array (Figure 4.3). Both arrays showed complete removal of all electrode tip IrO_x originally exposed through PPX-C by the deinsulation process. Pitting and etching of silicon at exposed tips was apparent for both devices as well, in many cases undercutting IrO_x that remained on electrode shafts underneath residual PPX-C. Cross sections through tip metal showed dendritic IrO_x structure expected of our reactive IrO_x sputtering process, suggesting little physical damage or change to metal that remained on electrodes. Curiously, the sciatic explant cross section showed silicon pitting underneath iridium oxide film covered by PPX-C, while the same was not seen for the femoral explant cross section.

Although similar observations of tip metal and silicon were made between USEAs, distinct PPX-C damage modes were seen for the two arrays. Both devices exhibited roughened PPX-C with fissures that completely penetrated the film, but the femoral explant in general displayed continuous PPX-C coverage of electrodes across the entire array. PPX-C thickness for this device measured via FIB cross section showed that evidence of the original 2.8 µm thick film remained, despite film roughening and fissure formation. In contrast, the sciatic explant showed exposure of silicon along the shaft or at the base of electrodes due to complete removal of PPX-C. Interestingly, residual PPX-C for most sciatic explant electrodes was present on electrode metal that was not originally exposed during oxygen plasma processing, although close observation of this film revealed completely penetrating cracks and craters (Figure 4.3(d)). Backscatter

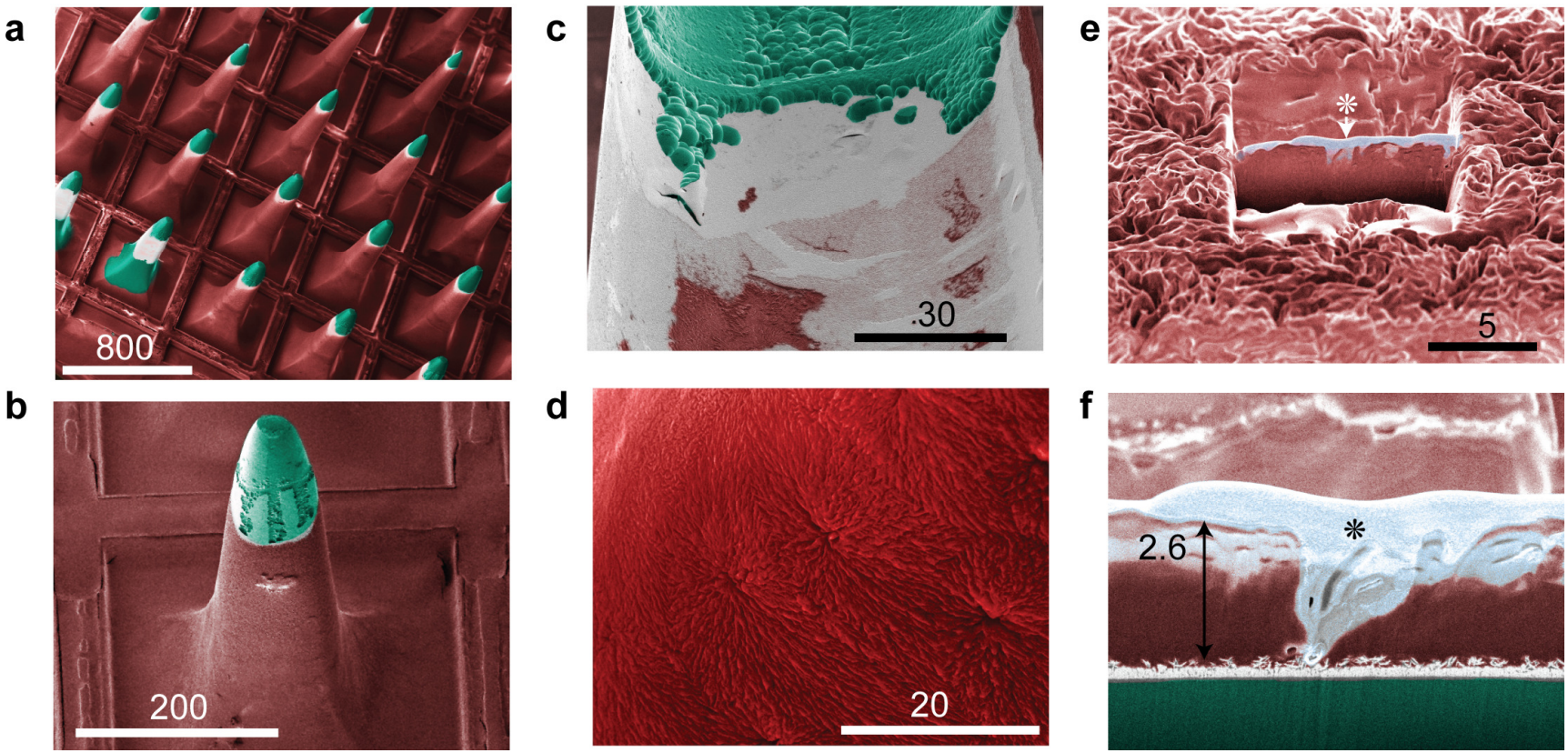

Figure 4.2 Images of USEA explanted from feline femoral nerve. Scale bars and values are in micrometers. (a) Array view of short-electrode region, showing consistent electrode tip damage. Lack of PPX-C on corner electrodes may be due to intentional manual removal of the PPX-C to generate on array reference electrodes prior to implantation. (b) View of single electrode, showing etching of silicon exposed around IrO_x metal. (c) Detail of electrode tip (distinct from electrode in (b) shows silicon pitting and some residual PPX-C, presumably after PPX-C degradation *in vivo*. (d) PPX-C over many electrodes showed surface degradation, but not complete erosion as seen in (c). (e) Considerable PPX-C surface topography visible around FIB cross section of parylene film over IrO_x on electrode shaft. (f) Full detail of cross section, showing PPX-C thickness varying from more than 2.6 µm to complete removal. For (e) and (f), light blue (marked with *) on top of parylene (red) is protective Pt deposited *in situ*. Blue-green – silicon; light gray – IrO_x.

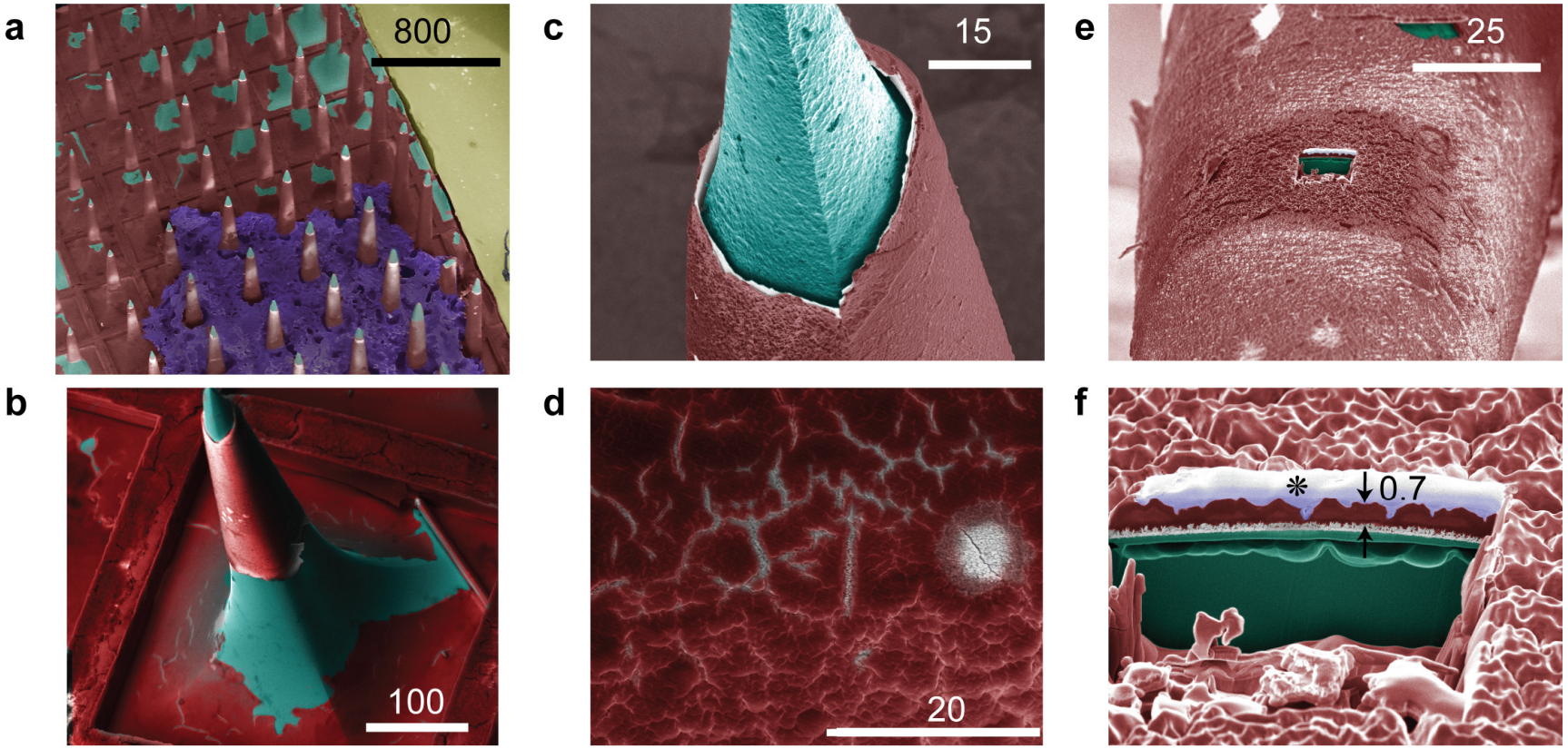

Figure 4.3 Images of USEA explanted from feline sciatic nerve. Scale bars and values are in micrometers. (a) Array view of long-electrode region, showing prevalence of electrode tip damage and PPX-C degradation. Residual tissue (purple) and silicone potting (yellow) of gold wires also shown (right side). (b) View of single electrode, clearly showing lack of tip metal and PPX-C destruction. (c) Electrode tip shows silicon pitting and undercutting of IrO_x/PPX-C film. (d) Detail of PPX-C over metal shows cracking and cratering. (e) Region of PPX-C along shaft that was subject to FIB cross-sectioning. (f) Detail of (e) shows extreme PPX-C surface topography, indications of silicon pitting/etching underneath IrO_x, and clear thinning of PPX-C with respect to 3 µm initial thickness. In (f), light blue (marked with *) on top of parylene (red) is protective Pt deposited *in situ*. Blue-green – silicon; light gray – IrO_x; yellow – silicone.

images showed reduced contrast between residual tip metal and PPX-C appearance on the sciatic explant, compared to PPX-C and tip metal on the femoral explant, indicating a thinned PPX-C film on the former. This was confirmed with FIB cross sectional measurements, which showed PPX-C thickness on the sciatic explant being less than 1 µm compared to the original 2.8 µm thick film.

None of the PPX-C degradation modes observed for explanted devices were visible on the soak test control electrodes, which were aged in heated PBS alone. A representative control array from the soak testing is shown in Figure 4.4(a), where the PPX-C film is observed to be completely intact. In general, no change to PPX-C film on controls was observed before or after aging, neither to the surface morphology nor to the bulk integrity. One control array out of six processed at 87 °C did exhibit nearly imperceptible PPX-C cracking, which became more visible after electrode charging from the primary electron beam during EDS measurements (Figure 4.4(b)). This was our first observation of PPX-C crack formation after aging in PBS, and the temperature at which it occurred (87 °C) is higher temperature than temperatures used in prior aging protocols. Prior studies of UEAs aged at 67 °C in PBS by our group, both published [18] and unpublished (>10 arrays total), have never recorded PPX-C crack formation solely due to aging in PBS. However, the addition of H_2O_2 to PBS aging at 67 °C was associated with PPX-C crack formation in six out of six UEAs (see Figure 4.4(d)-(g)). Damage manifestation varied across devices, ranging from sparse cracking that did not seem to penetrate the film (one array), to widespread damage (three arrays) and even signs of erosion (two arrays). PPX-C cracking for one UEA was accompanied by IrO_x delamination (Figure 4.4(f)). Close inspection of the film surface for these arrays

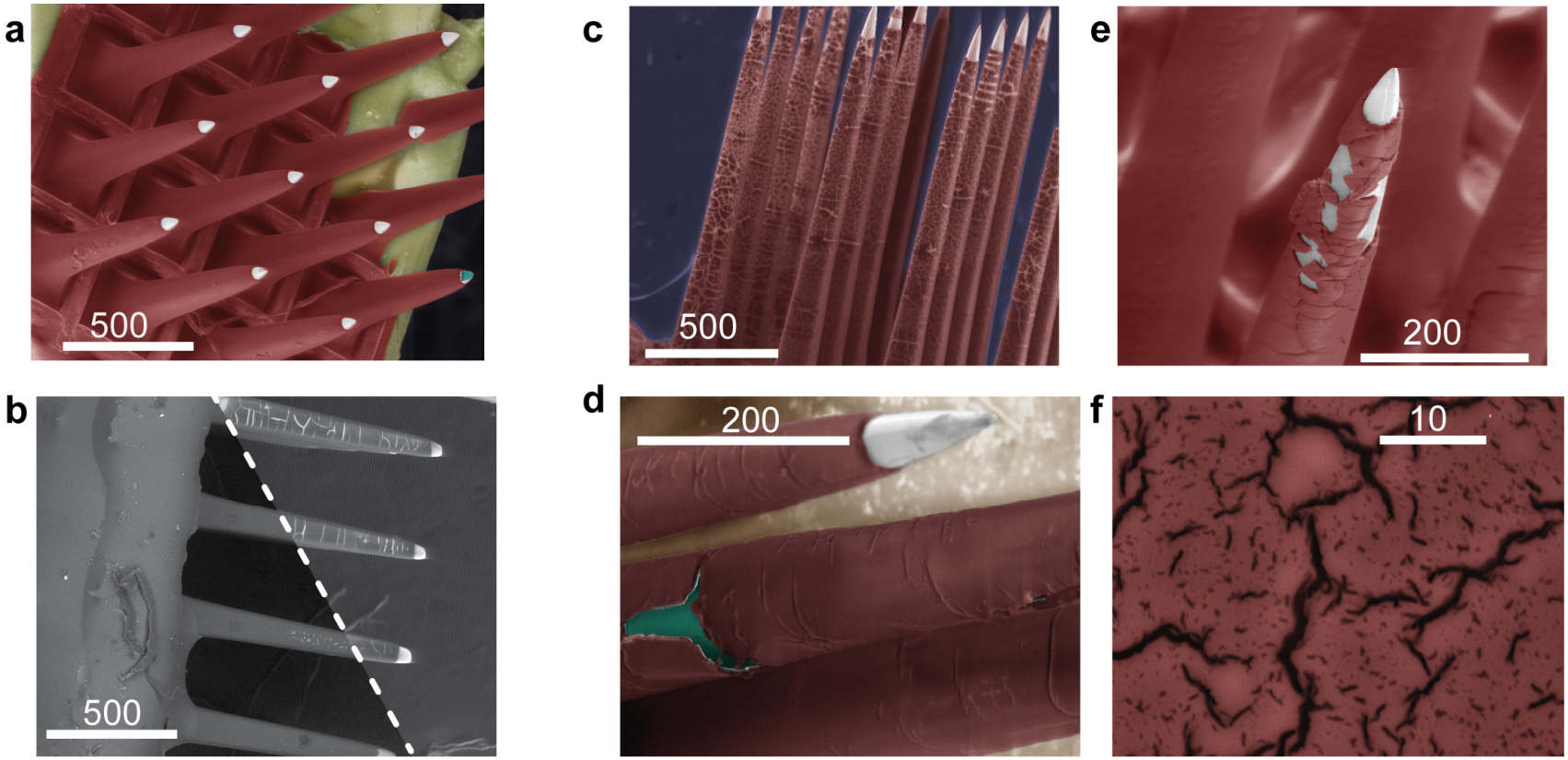

Figure 4.4 Representative SEM images of control UEAs subject to processing in PBS alone (a-b), and devices subject to RAA at 67 °C (c-f). Scale bars are in micrometers. (a) Typical control arrays showed no damage to PPX-C after aging in heated PBS. (b) One control array aged at 87 °C did show almost imperceptible cracking, not visible with backscatter imaging (left of dashed line) but apparent with secondary electron imaging (right) after considerable charging during EDS measurements (not colored to show contrast change). (c) Arrays aged in RAA at 67 °C consistently showed cracking of PPX-C. (d) Tip detail showing cracking and evidence of PPX-C removal. (e) One array showed cracking and delamination of IrO_x metal. (f) Detail image of PPX-C cracks. Colored images: red – parylene C; blue-green – silicon; light gray – IrO_x; yellow – silicone.

revealed frequent and variously-sized fissures, but little evidence of general surface roughening as was observed from the cat sciatic explants.

Arrays subject to RAA at 87 °C displayed the largest variation in endpoint appearances of all cohorts (see Figure 4.5). Out of 14 total arrays, two displayed moderate cracking, which did not proceed to the extent observed for most devices RAA-processed at 67 °C and are shown in Figure 4.4 (c)-(f). Parylene surface degradation was present for at least three arrays, appearing as a film roughening accompanied by obvious thinning in several cases. Figure 4.5(d) shows an example of cracks and craters accompanying degradation, not unlike that of the sciatic explant in Figure 4.3(d). Five arrays showed large-area removal of PPX-C, also similar to the sciatic explant. Curiously, the remaining four arrays in the 87 °C RAA cohort did not show obvious signs of PPX-C damage. Figure 4.5(e) shows surface detail and PPX-C cross section of one such array, revealing moderate topography and the full expected PPX-C thickness of ~6 µm. This is in contrast to a device processed concurrently which showed parylene thinning and removal (Figure 4.5(f)). Surface topography for this array was considerably rougher compared to the undamaged device, and cross sectioning revealed more than 75% loss in film thickness compared to the as deposited PPX-C film thickness. Voids in PPX-C were also visible at the parylene-silicon interface.

Although considerable and varied degrees of PPX-C damage occurred on UEAs aged under both RAA conditions, test structures aged concurrently did not exhibit the same degree of damage, and some had no discernable degradation (not shown). IDEs aged in RAA at 87 °C displayed PPX-C blistering and delamination, but no signs of cracking or surface damage. Similarly, no cracking or surface damage was seen on t-

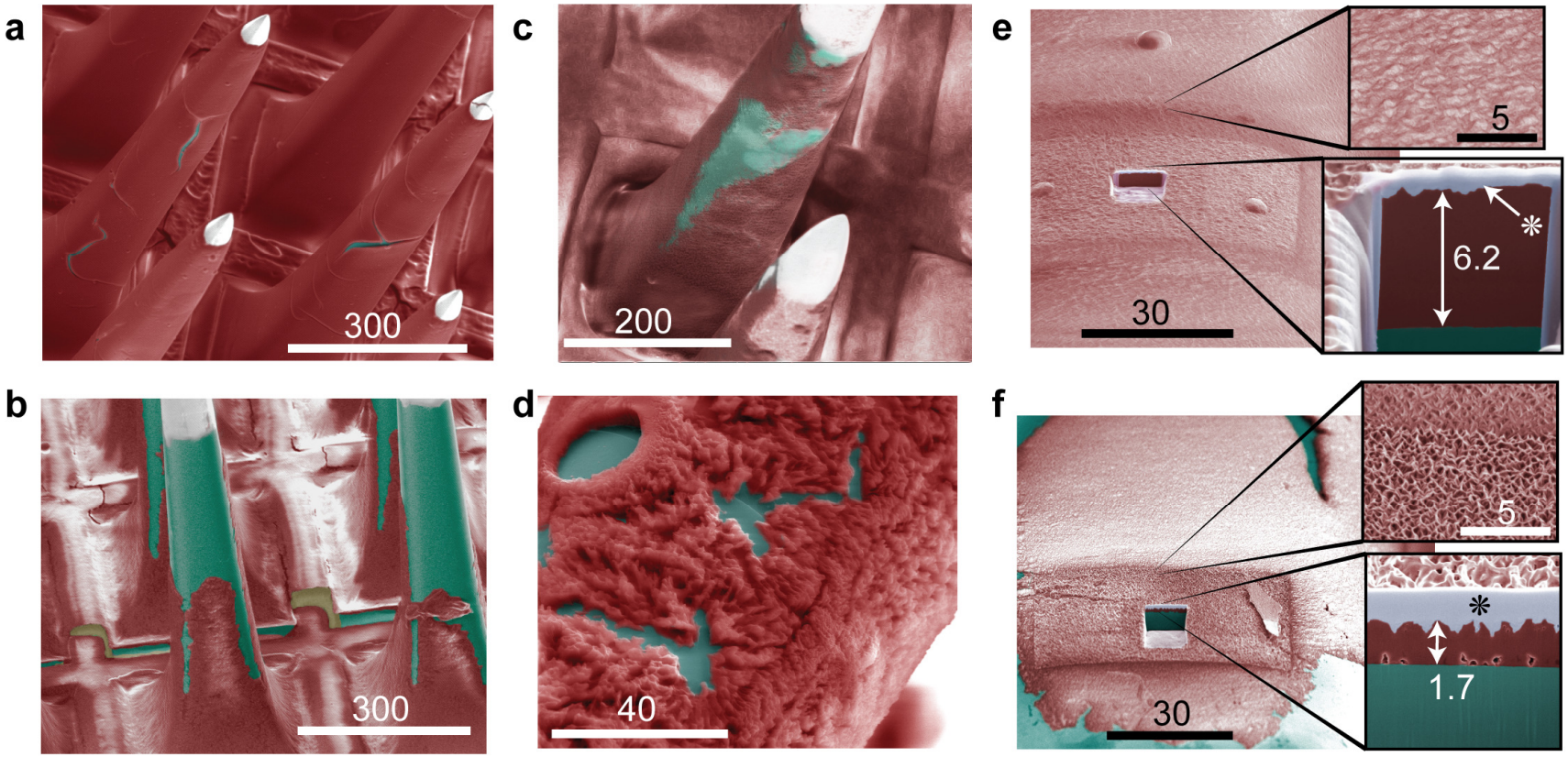

Figure 4.5 SEM images of arrays subject to RAA processing at 87 °C. Scale bars and measurements are in micrometers. Each image is representative of a different array and shows the diversity of results from high temperature RAA. Results varied from (a) moderate PPX-C cracking to complete degradation and removal, with (b) showing erosion presumably originating at the tip and moving towards the base, and (c) showing bulk thinning and removal. (d) Detail PPX-C damage over silicone, showing cratering and surface degradation not unlike that seen for *in vivo* arrays. (e) An array that did not show obvious signs of damage displayed moderate surface topography and PPX-C thickness similar to the as-deposited film. (f) An array that showed obvious PPX-C erosion displayed obvious irregular PPX-C topography and thickness reduction by at least 75%. For (e) and (f), light blue (marked with *) on top of parylene (red) is protective Pt deposited *in situ*. Blue-green – silicon; light gray – IrO_x.

UEA shafts aged in any condition. Prior reports have never noted PPX-C degradation on IDEs aged in PBS at a variety of temperatures [27], [50], nor on fully encapsulated (*i.e.* tips not exposed) UEAs [18]. The primary difference for t-UEA processing is the lack of exposure to O_2 plasma as part of the tip deinsulation process. These results suggest that oxygen plasma deinsulation of UEAs may play a role in reducing PPX-C robustness, but other factors such as the temperature during the process, and other mechanisms, have not been systematically ruled out.

4.4.2 Electrochemical impedance spectroscopy

EIS provided quantitative evaluation of electrode damage, complementing the qualitative characterization of electron microscopy. Impedance measurements for explanted arrays were limited to data taken at 1000 Hz, restricting comparisons between explants and *in vitro* devices. Sciatic and femoral arrays showed pre-implant average moduli of 190 and 263 kΩ, respectively. After implantation, impedance for these arrays increased respectively to 280 and 565 kΩ. Impedances continued to increase throughout the indwelling period, and sciatic array electrodes averaged 700 kΩ prior to explantation at the 3.5-year time point. Over 40% of these electrodes showed final measurements of >1000 kΩ, up from <5% of electrodes at the 0.75-year time point. The electrodes of the femoral array averaged 1700 kΩ prior to explantation, with 88% of electrodes showing values over 1000 kΩ after 3.5 years, compared to 40% after 0.75 years.

Physical characterization of the explants suggests the impedance increases for these arrays were driven by damage to electrode metal. The electrode metal deposition process has undergone changes since the fabrication of these implanted arrays, and these

modifications have decreased tip impedance mean and variance, as well as improved metal robustness. This improved metal was employed on our test arrays, which exhibited impedances almost two orders of magnitude lower than implants (3-8 kΩ at 1000 Hz), as well as very little metal damage during aging. While improved fabrication processing may have contributed to positive aging outcomes for metal, an additional consideration is the inability of the RAA system to model tip degradation mechanisms observed *in vivo* (*i.e.* silicon etching and metal undercutting).

The impedance spectra for devices aged *in vitro* generally correlated with the extent of PPX-C damage. Control arrays aged at 67 °C, for which no damage was observed, did not exhibit strong evidence of impedance change. This is consistent with previous reports of UEA impedance undergoing little change after aging in PBS at 67 °C for durations in excess of 100 days [18]. Half of 87 °C controls showed no impedance change (representative data shown in Figure 4.6(a)), with two devices showing slight impedance reductions across the spectrum, and one device showing increased 1000 Hz magnitude but reduced 1 Hz magnitude.

Most UEAs subjected to RAA exhibited impedance reduction, as has been previously reported for devices aged using RAA [21]. Examples of such impedance changes are shown in Figure 4.6(b)-(d), which illustrate distinct trends in impedance reduction based on severity of PPX-C damage. These are in contrast to a control device (no H_2O_2) that showed no damage or impedance change (Figure 4.6(a)).

Impedance reductions were observed at frequencies >1000 Hz for the mildly damaged case. Spectral changes transitioned to be most pronounced at frequencies <1000 Hz for cases of complete PPX-C removal. Figure 4.6(e) shows post-aging impedance of

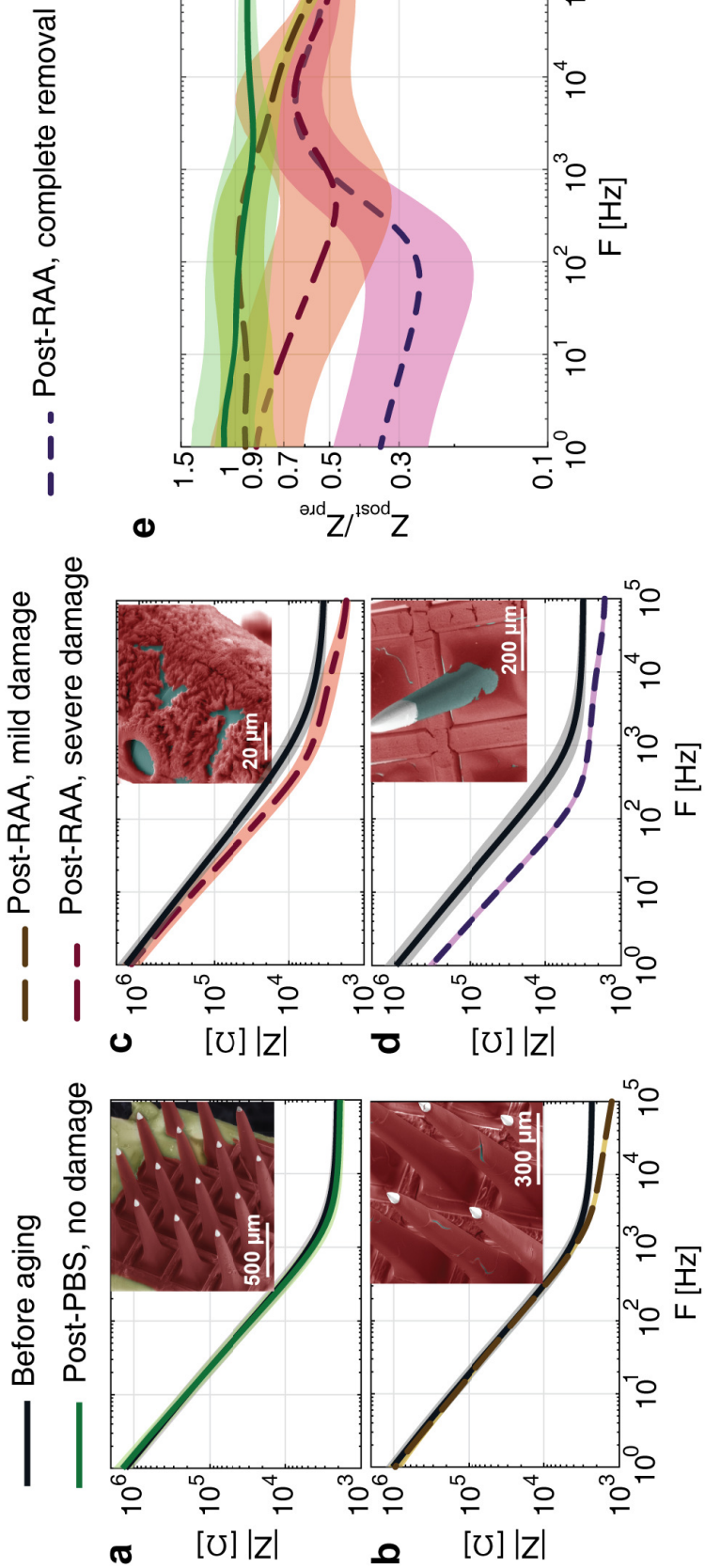

Figure 4.6 EIS results showing changes to EIS spectra commiserate with PPX-C damage. Insets are images of arrays from which spectra were taken. (a) No visible damage to PPX-C was seen for a control array aged at 87° C, corresponding with no meaningful change to impedance magnitude spectra. All remaining arrays were RAA-processed at 87 °C. (b) UEA with cracked parylene showed impedance reduction at frequencies >1000 Hz. (c) Degradation to parylene and more comprehensive shaft exposure from underneath encapsulation was accompanied by impedance reduction at 1000 Hz and below. (d) Full removal of PPX-C caused full-spectrum impedance reduction most pronounced at frequencies <1000 Hz. (e) Post-aging impedance normalized to initial values show how impedance change progressed across frequencies according to PPX-C damage mode. All plots are geometric averages of N=16 electrodes, shading indicates geometric standard deviation.

all four arrays, normalized to initial values. Impedance reduction at 10^5 Hz was seen to be sensitive to initial parylene damage, but changed very little as damage became more pronounced. Normalized impedance change at 1000 Hz was equal between the undamaged and mildly damaged cases, as well as between the cases of severe damage and complete removal. Impedance change became most pronounced at 100 Hz when most parylene was removed.

Damaged devices in Figure 4.6 were taken from the 87 °C RAA cohort, reflecting the diversity of impedance characteristics seen for that group. Almost all devices within this cohort showed clear evidence of impedance reduction according to the condition of the PPX-C coating. One device that maintained impedances close to initial values had sustained minor cracking that did not completely penetrate the PPX-C film. Five out six devices subject to RAA aging at 67 °C displayed full spectrum impedance reduction similar to Figure 4.6(d), which may be attributed to the considerable PPX-C cracking sustained by these devices.

4.4.3 Overview: absorption and emission spectroscopy

Absorption and emission spectroscopy modalities showed several clear and consistent trends, including strong oxygen content of *in vivo* samples and increased oxygen content of UEAs aged *in vitro* compared to untreated films. Results from each modality are discussed in the sections that follow, with modality-specific sample numbers shown in Table 4.3. Sample number nonuniformity was due to obstacles and constraints encountered while developing and executing these characterization methods, the use of which is novel for UEAs. For brevity, detailed EtO and EtO+ENZOL reference sample

Table 4.3

EDS, XPS, FTIR sample numbers by device group.

Device type	Processing condition	Sample number (N)		
		EDS[a]	XPS[b]	FTIR[b]
Aged UEAs	*In vivo*	12	2	4
	PBS, 67 °C	14	1	4
	PBS, 87 °C	15	3	4
	RAA, 67 °C	18	1	4
	RAA, 87 °C	20	3	4
Aged test structures	PBS, 67 °C	12	0	4
	PBS, 87 °C	6	0	1
	RAA, 67 °C	9	0	1
	RAA, 87 °C	10	0	4
UEA references	No deinsulation	6	1	1
	Deinsulation	10	1	2
Planar references	Oxidized	10	2	4
	O_2 etched	3	1	1
	Untreated	6	1	4

[a]N is sum of 2-3 measurements per device, save *in vivo* samples.
[b]One measurement taken per device, save *in vivo* samples.

results are omitted from this report. No indication was found using EDS, XPS, and FTIR that such processing altered film properties versus untreated references, in agreement with previous work [56]. We are confident that the *in vivo* results presented herein are directly due to effects of chronic implantation.

4.4.4 Energy dispersive X-ray spectroscopy

EDS measurements indicated that oxygen at% increased due to aging *in vivo* and *in vitro*, as well as from elevated (>67 °C) temperature processes such as thermal

oxidation, plasma etching, and deinsulation. The concentration of oxygen in PPX-C was of particular interest, as physical damage to PPX-C and reduction of the impedance was correlated with aging in an oxidative solution, such as the PBS with 20 mM H_2O_2 used in these studies. Figure 4.7(a)-(d) shows means and standard deviations of oxygen at% normalized to carbon at% (O_{norm}) for four different device groups. Our decision to normalize to carbon content was based on the assumption that most oxygen incorporated into PPX-C film would be due to carbon oxidation, as opposed to diffusion of diatomic oxygen or film hydration. Results for *in vivo*, control, and RAA arrays are shown in Figure 4.7(a). Residual PPX-C on *in vivo* arrays exhibited O_{norm} levels of over 0.08±0.03, approximately 2× that of 87 °C RAA devices, the next closest group. RAA at both 67 °C and 87 °C was accommodated by >20% increases to O_{norm} compared to respective controls; however, this change falls entirely within the standard deviations of both device sets and may be attributed to measurement noise. A more striking trend was observed between control and experimental arrays aged at 67 °C and 87 °C, where O_{norm} levels associated with 87 °C processing increased by >70% over devices processed at 67 °C.

Measurements of test structures followed similar trends as arrays (Figure 4.7(b)), with samples that were RAA-processed at 87 °C showing on average 60% increase in O_{norm} compared to samples at 67 °C. Test structure controls aged in PBS at 87 °C did not meaningfully differ in O_{norm} from those of the RAA experimental group at the same temperature. Interestingly, O_{norm} values of 0.01-0.02 for test structures were 25-50% lower than those of arrays aged using respectively identical *in vitro* conditions.

One key difference between aged UEAs and aged test structures was that the deinsulation process was performed for the former, but not the latter. As PPX-C damage

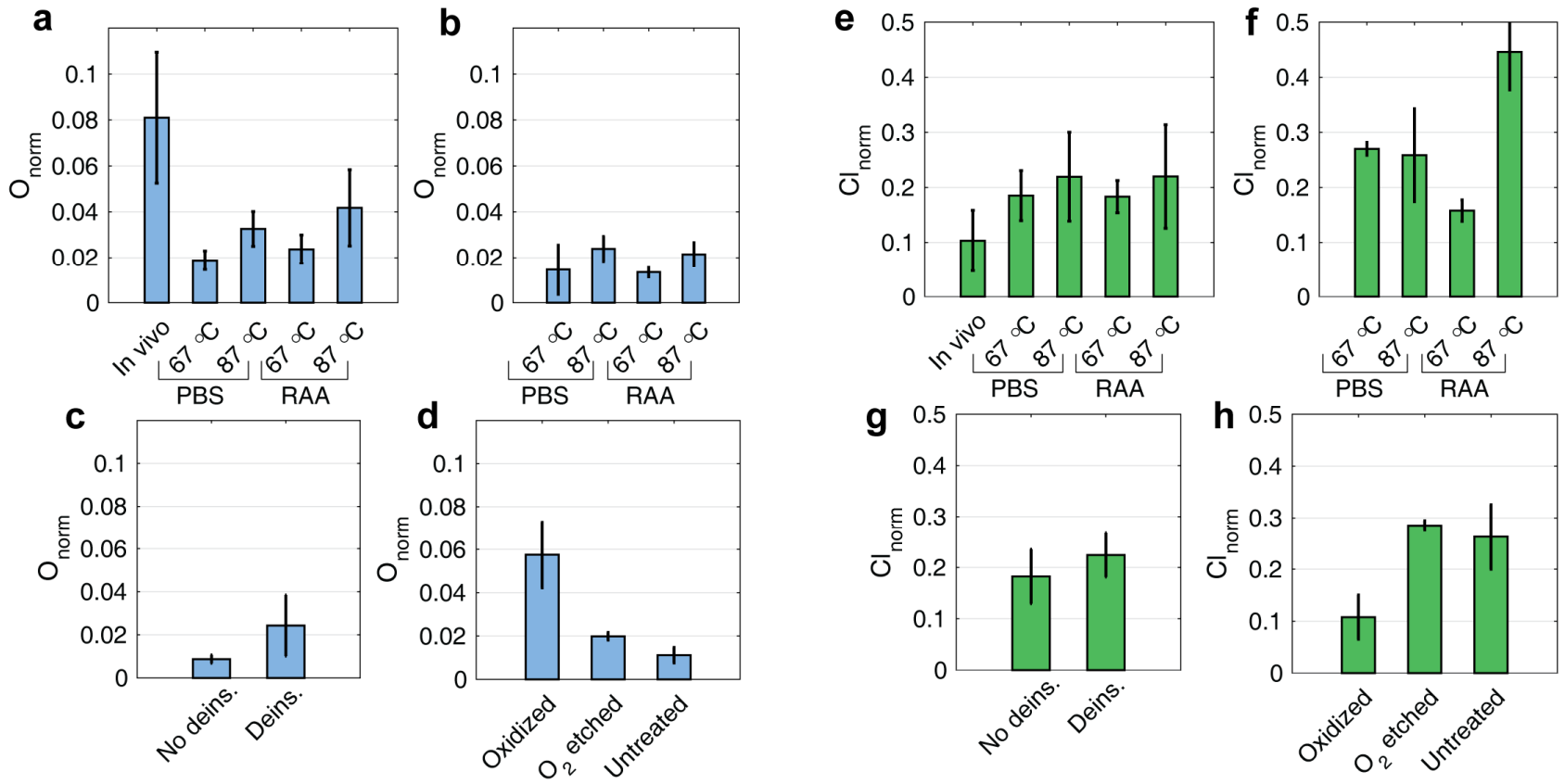

Figure 4.7 EDS permitted semi-quantitative characterization of PPX-C elemental composition. (a)-(d) At% of oxygen normalized to at% of carbon (O_{norm}) for (a) explant, control, and RAA arrays, (b) test structures (IDEs and t-UEAs), (c) reference arrays before and after oxygen plasma processing, and (d) planar reference samples. Bar graphs show mean and standard deviation. (e)-(h) Chlorine at% normalized to carbon (Cl_{norm}), shown in the same order as O_{norm}. (i) Markers illustrate where EDS spectra were taken for data in (j), which shows EDS intensity of PPX-C on an 87 °C RAA array, presumed PPX-C on the sciatic explant, and organic tissue on the sciatic explant. High-resolution plots show details for detected peaks, vertical dotted lines indicate associated X-ray energies used for peak identification.

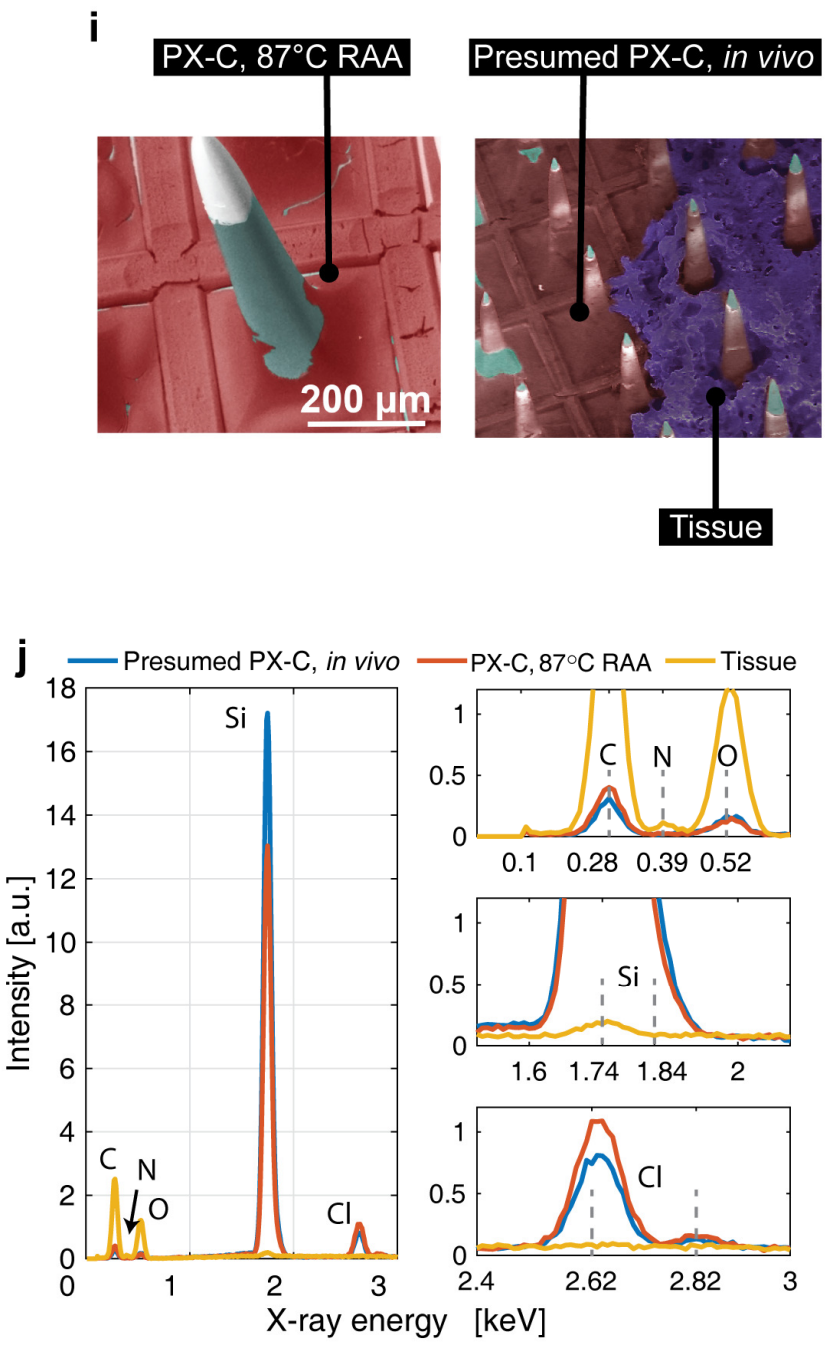

Figure 4.7 Continued

and elevated O_{norm} were associated with both deinsulated and aged devices, we conducted measurements of reference arrays without and with deinsulation to obtain preliminary data on the effect of deinsulation on the composition of PPX-C. Figure 4.7(c) displays these measurements, which suggest an increase in O_{norm} following deinsulation. One UEA measured with EDS before and after deinsulation showed a very distinct increase in O_{norm}, but for other devices no significant change was observed. This is reflected by the coefficient of variation (CoV) of 58% for deinsulated devices.

Planar reference samples subjected to known oxidative damage mechanisms were characterized to assist our understanding of how *in vivo* and RAA damage might be occurring. EDS of PPX-C on polished silicon substrates subjected to thermal oxidation, oxygen plasma etching, or no treatment (control) are presented in Figure 4.7(d). Thermal oxidation has been reported to be associated with carbonyl bond formation on aliphatic parylene linkages, leading to chain scission [38], [57], and average O_{norm} for these samples was approximately 0.06±0.02, which was between measurements for arrays aged *in vivo* and in 87 °C RAA. Oxygen plasma damage has been suggested to occur via benzene ring opening [55], [58], and yielded O_{norm} of 0.02±0.002, which was closest to control arrays aged at 67 °C and 75% larger than O_{norm} of untreated PPX-C. An increase in EDS-measured oxygen content after oxygen plasma exposure is consistent with previous work [59].

Evaluation of chlorine content normalized to carbon (Cl_{norm}) is shown in Figure 4.7(e)-(h). While stoichiometric PPX-C is characterized by a Cl_{norm} of 0.125, Cl_{norm} calculated from measurements of pristine PPX-C taken from non-deinsulated UEA and planar untreated references was 0.18±0.05 and 0.26±0.06, respectively. This discrepancy

underscores the semi-quantitative nature of EDS, and the Cl_{norm} range of 0.18-0.26 was taken as representing the unaged and undamaged condition against which all other devices were compared. *In vivo* samples showed Cl_{norm} values below this range (0.10±0.06), while arrays aged in PBS and per the RAA protocol exhibited Cl_{norm} between 0.18 and 0.22, with no temperature or H_2O_2-dependent trends seen. These results suggest that the films were adequately rinsed to remove salts from the physiological solution, which could serve to increase the Cl concentration. Measurements of test structure controls aged in PBS also fell within the range of unaged devices. However, RAA-processed test structures showed Cl_{norm} values in excess of 0.26, perhaps due to insufficient device cleaning after aging. Cl_{norm} for thermally oxidized planar references was similar to that of UEAs aged *in vivo*.

While conducting EDS and other spectroscopic measurements, there was concern that the film on *in vivo* arrays that was assumed to be PPX-C was in fact residual organic material. To increase confidence that the *in vivo* measurement we were taking were in fact of PPX-C, we compared EDS spectra of the parylene film in question to known parylene and organic sources. Figure 4.7(e) indicates where measurements were made for comparison. An array aged with RAA at 87 °C was chosen as a parylene reference due to the presence of RAA-induced thinning and surface damage similar to that seen on the sciatic explant. The organic reference signal was taken from the residual organic material on the sciatic explant, and the *in vivo* parylene signal was taken from presumed PPX-C film on the same explant. Figure 4.7(f) shows all raw spectra overlaid. Considerable similarity was observed between the known and presumed PPX-C films, made more apparent in the detailed spectra to the right of the full spectrum plot. The chlorine peak in

particular provided a telling indication of PPX-C film, as it was completely absent from the spectrum of the known biological material. From these data, we are confident that measurements taken from *in vivo* arrays are in fact of PPX-C and not tissue residue.

4.4.5 X-ray photoelectron spectroscopy

XPS measurements of surface composition were similar to EDS measurements. However, unlike EDS for which several measurements could be made at different sites for the same array/device, XPS measurements required sampling a larger surface area, such that only one independent measurement was possible for each sample. Sputtering cleaning with an argon ion beam was performed to remove possible surface contamination and extended for depth profiling after as received measurements were collected. This permitted multiple measurements across the same area, but also likely altered the PPX-C composition and chemical structure. An indication of measurement repeatability was obtained by duplicate analysis of four samples (one *in vivo*, two 87 °C RAA arrays, one 87 °C PBS control array), without argon sputtering. CoVs for O_{norm} and Cl_{norm} did not exceed 40% for all devices, and were commonly 15-25%, with inter-device trends largely maintained across measurements. Analysis of carbon binding to oxygen was less repeatable, with one sample showing a CoV of 80%. Therefore, for improved confidence as well as ease of comparison to EDS data, most XPS data analysis was focused on elemental composition measurements. These data are shown in Figure 4.8, for which measurements are grouped by aged arrays (Figure 4.8(a), (d)), reference arrays (Figure 4.8(b), (e)), and planar references (Figure 4.8(c), (f)). Regarding sample counts (see Table 4.3), the repeated measurements previously mentioned were averaged to give

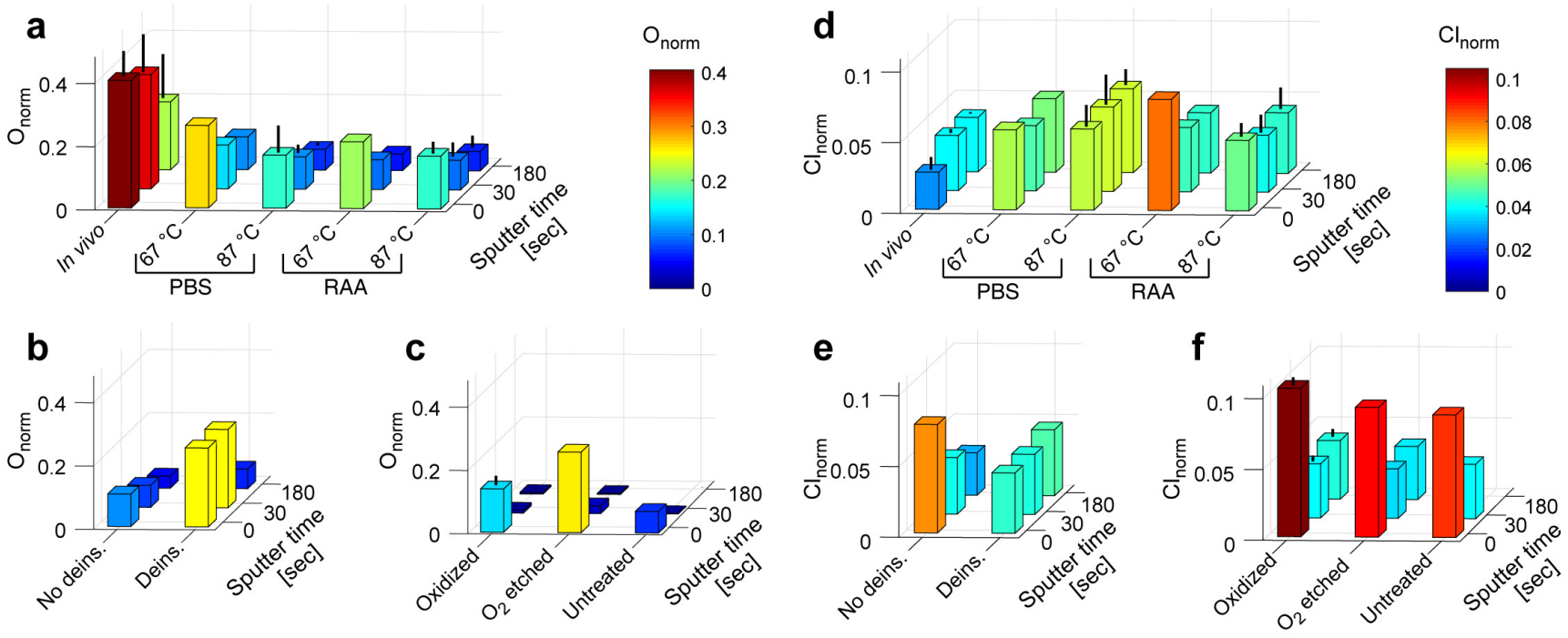

Figure 4.8 XPS data areshown as O at% (a)-(c) and chlorine (d)-(f) for different devices normalized to carbon at%. Bar colors correspond to normalized values as shown by color scales. Where present, error bars indicate standard deviations between measurements of different samples. Sputter time refers to surface sputtering with an argon ion beam, which removed adventitious carbon, other physiosorbed species (*e.g.* O), and a small amount of the surface material, and enabled depth profiling with longer etches. Region scans of the as received carbon envelope shown in (g)-(i), corrected for Shirley background signal, permitted visualization of high-energy tails associated with carbon bonding to chlorine and oxygen. Legend identifies Gaussian-Lorentzian fits generally in order of lowest to highest binding energy. (a), (d), (g) Aged UEAs; (b), (e), (h) reference UEAs; (c), (f), (i) planar reference samples.

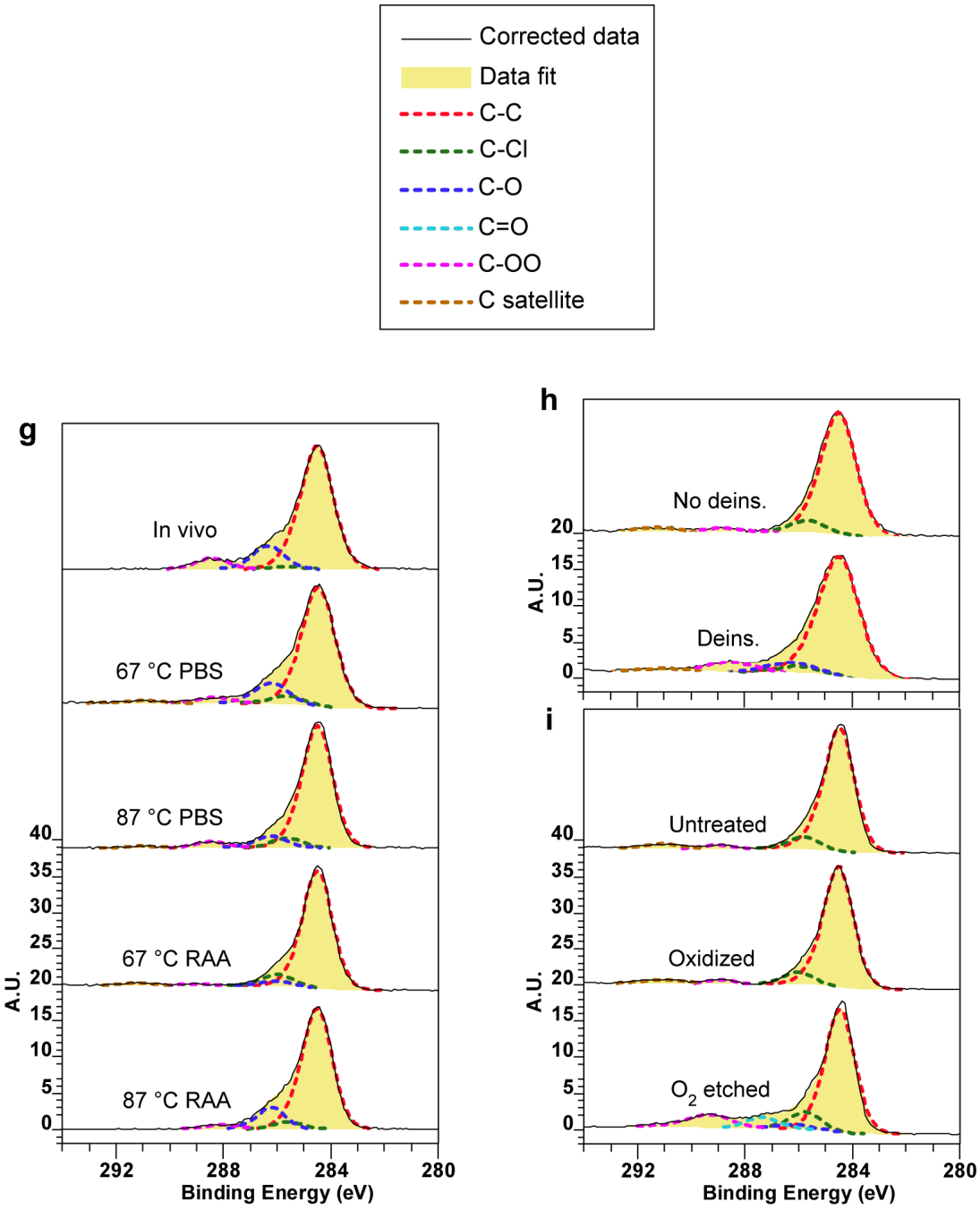

Figure 4.8 Continued

an N of 1 for each sample analyzed in duplicate. These means were then averaged with measurements of other samples from matching cohorts to give cohort means and standard deviations, for sample groups of N>1.

Similar to EDS measures, average as-received XPS measures of O_{norm} for UEAs aged *in vivo* (0.40±0.08) was the highest among all groups, being more than 2× that of arrays RAA-aged at 87 °C (0.17±0.03). Little difference in O_{norm} was seen between RAA and control measurements for a given temperature. PPX-C on all aged devices exhibited higher average O_{norm} than pristine PPX-C on non-deinsulated UEA and untreated planar references, which showed O_{norm} = 0.10 and 0.07, respectively, slightly higher than values reported elsewhere [60], [61]. Deinsulated UEA and O_2 etched planar reference results both showed increased O_{norm} compared to untreated samples, being 0.25 for both, which is consistent with prior characterization of oxygen-plasma etched PPX-C [61]. Also similar to EDS, *in vivo* samples showed the lowest Cl_{norm} of 0.026±0.007.

Unlike EDS results, however, higher aging temperatures were not correlated with higher O_{norm}. As-received XPS results indicated the opposite, with aging at 67 °C having higher O_{norm} than aging at 87 °C. In another reversal from EDS trends, higher O_{norm} was measured for oxygen plasma-processed planar reference sample compared to thermally oxidized references (O_{norm} = 0.14±0.03). Thermally oxidized samples also exhibited the highest Cl_{norm} of 0.10±0.01 according to XPS, while the same samples showed one of the lowest Cl_{norm} according to EDS. Cl_{norm} measurements for untreated and O_2 plasma-treated reference samples were slightly lower than oxidized references and within 5% of each other, in contrast to Cl_{norm} of non-deinsulated and deinsulated arrays that differed by 44%. The information depth of XPS measurements is ~5 nm, compared to the ~1 µm

information depth for EDS measurements, which is potentially one difference in the measurements. Argon beam sputtering of samples tended to change the measured compositions, which after sputtering became more similar to untreated PPX-C references. O_{norm} for all devices decreased with sputtering, with array measurements reaching similar values to those of the non-deinsulated UEA, and processed planar references decreasing to similar levels as the untreated planar reference. The *in vivo* array was a notable exception, maintaining higher O_{norm} levels than all other devices at all stages of sputtering. The after-plasma treatment reference array also demonstrated little change and the second largest O_{norm} after 30 seconds of sputtering; however, after 180 seconds it was similar to non-explanted devices. These results suggest that while oxidative changes to PPX-C during chronic implantation may penetrate the bulk, oxidation of PPX-C remaining after *in vitro* aging may be limited to the surface. Plasma processing of arrays may incur deeper changes to the PPX-C coating, but this must be verified in future work.

Measurements of Cl_{norm} after 30 seconds of sputtering were near 0.04 for all samples save UEA controls aged at 87 °C, which were closer to 0.06; these values changed little after 180 seconds of sputtering, and are less than 50% of the expected stoichiometry (0.125). This discrepancy may reflect a combination of effects arising from impure PPX-C dimer (known to contain a certain amount of parylene N due to manufacturing limitations) and local chemical changes due to ion bombardment. We note that evidence of Cl^- ions was apparent for *in vivo* arrays and UEAs aged at 87 °C (both PBS and RAA), and was accompanied by sodium peaks in the survey scans for these devices both before and after sputtering. Sodium and Cl^- were not detected for any other samples, and are potentially attributed to ion permeation of the PPX-C film during aging.

Therefore, actual carbon-bonded chlorine content for these devices is expected to be slightly lower than the Cl_{norm} levels reported in Figure 4.8(d).

Region scans of the carbon envelope between binding energies of 280 and 294 eV had high-energy tails associated with carbon oxidation, as seen for the examples shown in Figure 4.8(g)-(i). Spectra are presented with intensity normalized to the C─C peak at ~284.5 eV. All samples demonstrated indications of ─COO bonds, perhaps due to oxidation of unterminated PPX-C radicals [49], [62] or measurement noise. Intensity of presumed ─COO and ─CO binding was proportional to carbon envelop tail formation, with aged and plasma-processed devices having larger tails and higher oxidation intensities than untreated and thermally processed devices. Larger ─CO intensities were observed for UEAs aged *in vitro* and *in vivo* than for arrays processed in oxygen plasma, while the latter generally had higher ─COO intensity. Evidence of C═O chemistry and a strong carbon envelope tail were seen for the planar O_2 etched reference, consistent with prior work [61]. Carbon satellite peaks (C-satellite) attributed to benzene ring formation were near the noise limit for most devices, thus their presence was inconclusive.

4.4.6 Fourier-transform infrared spectroscopy

FTIR is sensitive to changing dipole moments associated with the vibrational characteristics of some chemical bonds, and provided an additional indication of PPX-C oxidation, which was clearly evident in spectra for *in vivo* UEAs and thermally oxidized samples. Representative examples of spectra from 3500-670 cm^{-1} (Figure 4.9(a)) had peaks near 1700 cm^{-1} for these devices, attributed to carbonyl bond formation [37], [57], [63]. The remaining samples lacked obvious signs of such oxidation, but shared many

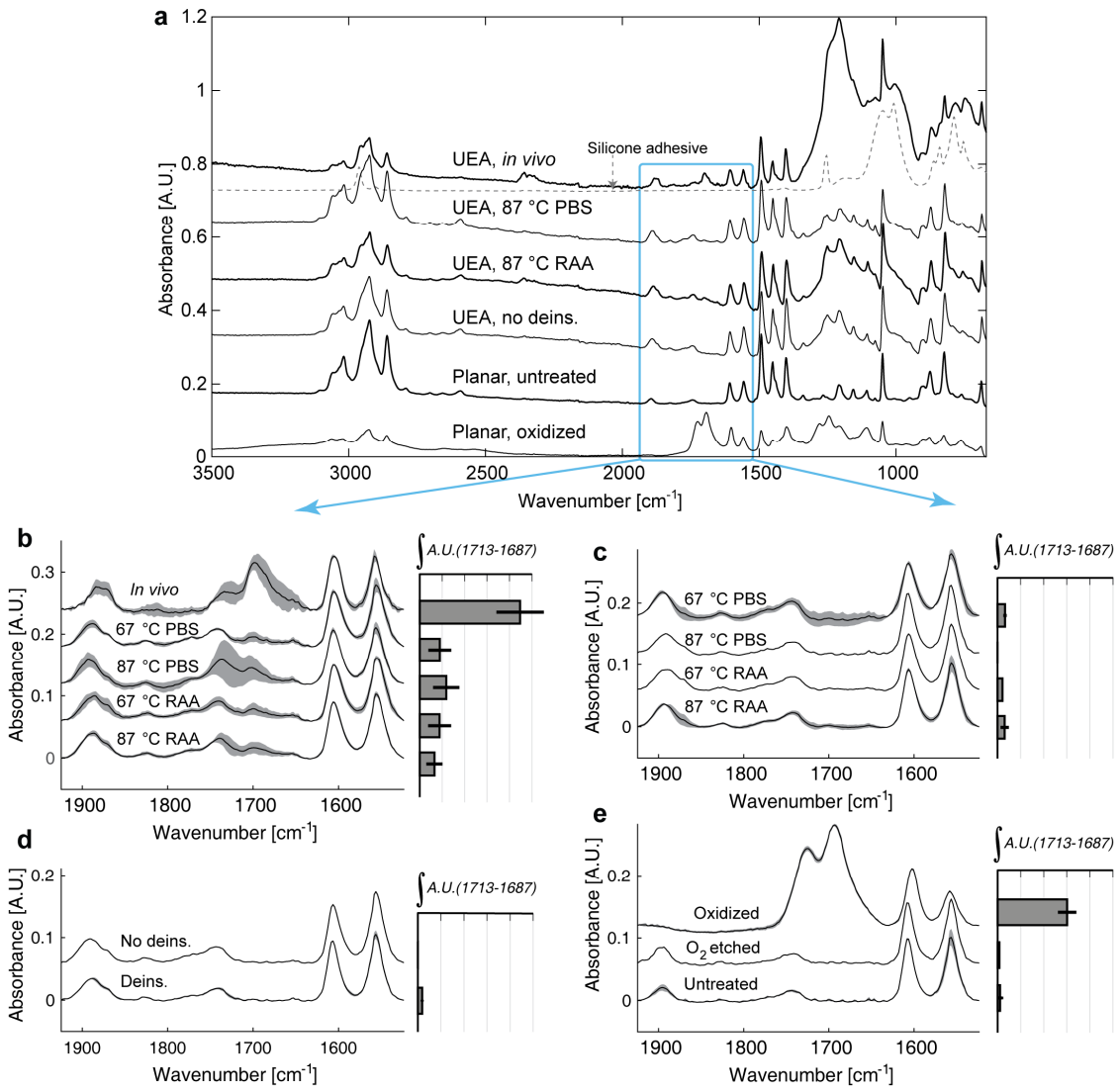

Figure 4.9 FTIR measurements provided an additional indication of PPX-C oxidation. (a) PPX-C scans from 650-3500 cm^{-1} are shown for representative samples. PPX-C from UEAs was placed on a silicone adhesive, the spectra for which is shown as a dotted line. Background silicone signal was evident for *in vivo* samples due to thinned (<3 µm) parylene film. The region from 1530-1920 cm^{-1} was analyzed for signs of film oxidation for all samples. Averages and standard deviations (where available) of normalized spectra are given for (b) aged UEAs, (c) aged test structures, (d) reference arrays, and (e) planar reference samples. Horizontal bars show area integrated within the window of 1713-1687 cm^{-1}, after baselining to window edges.

other spectral features, a selection of which are identified in Table 4.4.

Pristine PPX-C was represented by the planar untreated condition and was in agreement with previously published infrared absorption data [60]. Spectra of PPX-C from UEAs consistently differed from the planar untreated case due to the inclusion of a broad carbon-fluorine peak near 1250 cm^{-1}, a byproduct of the XeF_2 etching step require to extract PPX-C from the UEAs. This peak was particularly strong for the *in vivo* sample shown and may reflect a higher propensity for C─F reactions in highly damaged PPX-C films. Carbon dioxide absorption peaks near 2350 cm^{-1} for the *in vivo* spectrum likely arise from trace carbon dioxide within the FTIR instrument, which was artificially amplified during signal normalization owing to the small *in vivo* signal compared to other samples. Prominent C─F and carbon dioxide features were also observed in the spectrum shown for a UEA heavily damaged by RAA at 87 °C. Virtually no sign of water absorption was noted for aged UEAs, normally indicated by a broad peak formation between 3500-3200 cm^{-1} due to O─H stretching. Since water absorption by as-deposited

Table 4.4

Select FTIR peak assignments for PPX-C spectra.

Frequencies [cm^{-1}]	Assignment	Reference
3800-3100	Aromatic C─H stretch	[65]
1730-1690	C═O stretch	[37], [57], [63]
1600-1400	Aromatic C═C─C stretch	[65]
1275-1230	C─F stretch	[59], [66]
1050-1045	Aromatic C─H bend	[65]

PPX-C is known to occur and be detectable by FTIR [64], we suspect that exposure of our samples to high vacuum during prior characterization steps resulted in evaporation of a significant amount of the absorbed water.

The silicone adhesive used in mounting UEA PPX-C contributed to FTIR background for some devices, particularly *in vivo* samples due to parylene thickness being <3 μm (similar to or less than FTIR probe depth) for these samples. Therefore, interpretation of spectra at frequencies <1120 cm^{-1} was complicated by the presence of artifact peaks from the silicone. Silicone was the selected adhesive due to a flat FTIR spectrum at frequencies above 1500 cm^{-1}, permitting artifact-free comparisons of PPX-C oxidation as interpreted by quantification of the carbonyl peak [37], [57].

To make these comparisons, a two-part piecewise baseline that linearly interpolated between absorbance values at 1925, 1630, and 1524 cm^{-1} was subtracted from each spectrum. Baselined spectra were normalized to the integral of the peak between 1630-1580 cm^{-1}, which was largely conserved between all samples, and averaged between cohorts. Averages and standard deviations (where available) of thus-corrected 1925-1524 cm^{-1} spectra for devices are shown in Figure 4.9(b)-(e).

As previously noted, oxidation of *in vivo* samples (shown in Figure 4.9(b)) was correlated with a peak at 1697 cm^{-1}, between prior reported carbonyl peak values for PPX-C of 1701 cm^{-1} [63] and 1695 cm^{-1} [37], [57]. Detailed observation of UEAs aged *in vitro* (RAA and PBS controls) also revealed signs of carbonyl peak formation, to a similar extent between all *in vitro* samples regardless of processing temperature or condition. The large standard deviation for PBS controls at 87 °C was caused by a sample with a local baseline offset, but which otherwise showed signs of oxidation similar to

other samples. Although the presumed carbonyl peaks for *in vitro* UEAs are small, they exist in contrast to most remaining samples. Aged test structures (Figure 4.9(c)) show very slight carbonyl peak formation, if at all, and the same is absent for unaged UEAs (Figure 4.9(d)) as well as all but oxidized planar references (Figure 4.9(e)).

The presence of carbonyl peaks was further quantified by integrating spectral absorbance between 1713 and 1687 cm^{-1}, after subtracting an additional baseline linearly interpolated between window boundaries. Horizontal bar graphs in Figure 4.9(b)-(e) show averages and sample deviations of these integrals for each device group. Peak areas of UEAs aged *in vitro* were over 2× those of test structures so aged, while carbonyl peaks for unaged, nonoxidized samples were smaller still. Quantification of carbonyl peaks for *in vivo* UEAs and oxidized planar references yielded areas at least 3× larger than UEAs aged *in vitro*. Thus, in this first reported use of FTIR to evaluate neural electrode encapsulation, we found strong signs of film oxidation incurred *in vivo*, as well as indications that *in vitro* processing of UEAs may also introduce oxidation to a degree, agreeing with EDS and XPS data.

4.4.7 Statistical analysis of EDS and FTIR results

Statistical testing of O_{norm} EDS data and FTIR peak areas between 1713 and 1687 cm^{-1} further verified observed oxidation trends in the data. Testing was not performed on XPS data due to insufficient sample sizes. However, devices were grouped into statistical cohorts according to trends in the spectra that were consistent with XPS results. Due to the lack of consistent trends based on processing condition (PBS versus RAA) or temperature (67 versus 87 °C), all *in vitro*-aged UEAs were combined in a single group,

as were all *in vitro*-aged test structures. The remaining groups were comprised of *in vivo* devices, non-deinsulated and deinsulated UEA references, and planar untreated parylene references (six groups total). Welch's ANOVA found statistical significance ($p<0.001$) between these groups for both EDS and FTIR data, and Games-Howell post hoc testing found *in vivo* devices to be significantly different from all groups, including *in vitro*-aged UEAs. Aged UEAs did show significantly higher FTIR-measured oxidation levels than all groups aside from *in vivo*, suggesting that *in vitro* accelerated aging may be able to approximate oxidation incurred *in vivo*. However, the significant difference between UEAs aged *in vivo* and *in vitro* emphasizes the need for further work to better understand the differences in chemistry between RAA and *in vivo*, and potentially improve the fidelity of the *in vitro* methodology to better represent *in vivo* processes.

4.5 Discussion

The failure of implanted neural interfaces has been attributed to neural electrode material damage, including degradation of dielectric encapsulation [28], [31], [43], [67]. Eliminating this failure mode requires knowledge regarding the nature of damage incurred *in vivo*, as well as relevant test methods that can evaluate new electrode designs and materials. To meet these needs, we have characterized silicon micromachined electrode arrays that have been aged *in vivo*, compared to existing and novel *in vitro* accelerated aging paradigms, focusing on how such aging affected PPX-C encapsulation. Using characterization methods never before reported for UEAs, we found strong evidence of oxidation to PPX-C film damaged *in vivo*, and that *in vitro* aging paradigms that include oxidative mechanisms may better represent observed degradation

mechanisms.

4.5.1 Characterization of *in vivo* damage to PPX-C

Two USEAs that were implanted in feline peripheral nerve for more than 3 years had severe damage to PPX-C based on SEM and characterization of the devices after explantation. The degradation included cracking, cratering, thinning, and complete film erosion. Spectroscopic characterization techniques were used to better understand any changes to PPX-C chemistry that may have contributed to this damage. Using EDS, XPS, and FTIR, we found consistent indications of elevated oxygen levels in PPX-C from implanted devices compared to controls and references. We also found evidence using EDS and XPS that the chlorine content was reduced for implanted devices. Similar results were observed for thermally oxidized PPX-C reference samples using EDS, FTIR, and to a more limited extent, XPS. These results strongly suggest that oxidative reactions contribute to *in vivo* damage mechanisms, likely arising from ROS generated by the immune respiratory burst and persistent oxidative stress.

To our knowledge, the post-explant conditions observed here represent the most extreme damage to PPX-C incurred *in vivo* reported to date, although considerable damage to other implanted dielectrics such as silicon oxide has been previously noted [16]. Prior reports of PPX-C damage to implanted neural electrodes have found cracking, thinning, and cratering after 3 years [31], as well as cracking and delamination after shorter time points [28]–[30], [43], although to a lesser extent than that noted here. One key difference between the UEAs of this study and previously reported devices is implant location. The USEAs examined for this report were implanted in peripheral nerve,

compared to cortex for many other reports. Oxidative stress is known to occur in both peripheral nerve and cortex in response to implant injury, and although no direct comparison of ROS production is known to exist in the literature, Christensen *et al.* noted similar inflammation timeframes for peripheral and cortical implants when studying the foreign body response to feline peripheral nerve [68]. The authors also noted that peripheral nerve regeneration occurred at the implant site, in contrast to cell death often noted in cortical implant regions, which has been attributed to oxidative stress [33], [34]. These data do not indicate heightened oxidative stress at peripheral implant sites compared to cortical implants, and in fact may suggest the opposite.

Physical movement may also contribute to implant damage discrepancy, as neural interfaces implanted within hind limb nerve are expected to experience more shearing motion against local tissue compared to the micromotion of cortical implants. This agitation could physically remove PPX-C on neural implants already weakened by film oxidation, which is known to reduce parylene tensile strength [63]. However, peripheral implants are commonly fixed in place using surgical techniques, which can be inadvertently assisted by the formation of fibrous capsules around the implant [68]. Furthermore, physical damage is expected to be nonuniform across different aspects of the device, preferentially occurring on edge electrodes with a lesser effect on center electrodes. However, no such trend was observed for the explanted devices analyzed here. Fully elucidating the nature of the damage we observed on explanted USEAs, as well as how representative it is of neural electrodes, will require deep analysis of more samples in addition to the two reported here. Such multiyear implantations are difficult experiments, thus characterization of the relatively few devices explanted after such long

time frames is of great value. Furthermore, the difficulty of chronic *in vivo* experiments drives the need for accelerated aging testbeds that can more efficiently evaluate new material robustness. Based on our results, the RAA method reported here is promising in that regard.

4.5.2 Characterization of *in vitro* damage to PPX-C

RAA processing at 67 and 87 °C for durations equivalent to 224 days at 37 °C based on (1.1) resulted in consistent damage to PPX-C not replicated by aging in PBS alone. RAA processing at 67 °C resulted in PPX-C cracking visible in at least 5 out of 6 UEAs. RAA processing at 87 °C induced aging effects including cracking, thinning, cratering, and complete removal, similar to topography observed on *in vivo* USEAs. In contrast, aging in PBS at the same temperatures yielded very little visible change to PPX-C, with only one UEA out of more than six processed showing signs of crack formation after aging at 87 °C.

We expected that differences in spectroscopic characterization would accompany the observed physical changes between RAA-processed UEAs and PBS controls. Impedance measurements indeed reflected physical damage to PPX-C, and RAA processing was commonly accompanied by impedance decreases throughout the measured spectrum. Impedances for devices aged in PBS changed little compared to RAA cohorts, agreeing with previous work [21]. However, differences attributable to RAA versus PBS processing were not apparent using EDS, XPS, or FTIR. All modalities showed heightened levels of oxygen in aged PPX-C films on UEAs compared to untreated, unaged PPX-C. EDS showed signs of temperature dependence on oxygen

concentration, which could be evidence of increased diffusion of water, dissolved gases, or a progression of oxidative reactions into the PPX-C at higher temperatures, but this trend was not repeated with XPS and FTIR measurements. XPS analysis of the carbon envelope and FTIR measurements from 1713-1687 cm^{-1} indicated that oxidation of PPX-C carbon bonds accompanied *in vitro* aging, regardless of H_2O_2 presence. This agrees with previous work that found increased oxygen concentration in PPX-C after immersion in 0.9% NaCl and artificial body fluids lacking obvious oxidative constituents [56].

Similar to UEAs, test structures showed no difference in oxidation level based on presence or absence of H_2O_2 during *in vitro* aging. EDS revealed a temperature-dependent trend in O at% as was observed for UEAs, but this could not be confirmed by other modalities. Strikingly, no physical damage was observed on test structures despite simultaneous RAA processing with UEAs that did experience significant degradation. This lack of damage was accompanied by reduced oxidation compared to aged UEAs measured by EDS and FTIR. We cannot attribute this difference to the as-deposited parylene film, since test structures and UEAs were coated with PPX-C within the same deposition run. The most notable differentiating factor between the two device sets was the O_2 plasma deinsulation process, which is a necessary step for UEA fabrication but was not used on test structures. This suggests that the oxygen plasma deinsulation procedure may play a role in PPX-C aging damage.

4.5.3 Effect of the deinsulation process on PPX-C

Observations of as-fabricated arrays before aging did not detect any sign of physical damage to PPX-C after deinsulation. We have on occasion noted crack

formation in PPX-C on deinsulated UEAs directly after production, leading to rejection of the devices for quality control. Interestingly, these devices would have likely passed traditional quality metrics such as impedance measurements and optical imaging. The operative assumption has been that PPX-C films that do not undergo visible changes during the deinsulation process have similar integrity to the as-deposited film. However, the spectroscopic characterization reported here of PPX-C on non-deinsulated and deinsulated UEAs suggest otherwise. EDS and XPS characterization found increased oxygen at% on films subject to deinsulation, at levels similar to those seen for deinsulated UEAs aged *in vitro*. FTIR also indicated increased carbonyl signal for PPX-C on deinsulated arrays compared to non-deinsulated UEAs, although this signal was much smaller than those of aged UEAs. In addition, XPS measurements noted loss of chlorine for a deinsulated device compared to a non-deinsulated reference. This information, taken into account with the observations of damaged PPX-C on aged UEAs but not on t-UEAs or IDEs, strongly implies that the UEA deinsulation process can incur changes to PPX-C which reduces resilience against aging.

PPX-C remaining on UEAs after deinsulation has historically been considered undamaged by oxygen plasma, due to the foil mask designed to protect the body of the encapsulated device. However, differences in PPX-C film chemistry were seen with EDS and XPS from before and after deinsulation, and deinsulation processing was correlated with RAA damage. Preliminary investigations have found temperatures within the plasma chamber can reach in excess of 100 °C, and the ambient in the chamber is pure O_2 with some radicals and reactive oxygen species generated by the plasma. Also, the elevated temperatures may alter the integrity of PPX-C that is masked from plasma by

aluminum foil. Heat treatment of parylene has been studied extensively, and is known to increase film crystallinity [53]. When performed in an inert atmosphere such as nitrogen, annealing and associated crystallinity changes have been noted to increase tensile strength [24], as well as reduce the rate of water diffusion through films [64]. Less advantageously, compromised substrate adhesion has been a noted byproduct arising from thermal mismatch between annealed parylene and its substrate [49], resulting in increased blister formation during soak tests [69].

In contrast, we and others have noted film embrittlement and cracking when parylene is heated in an oxygen-containing atmosphere [49], [70]. The oxygen pressure within the plasma chamber during deinsulation is 0.4 Torr, 0.25% that of oxygen in atmosphere. This alone combined with heat may not be sufficient to cause obvious oxidative damage on aluminum foil-masked PPX-C. However, the high reactivity of oxygen radicals within the active plasma chamber may unpredictably alter reaction kinetics during deinsulation to favor film oxidation. The oxygen plasma deinsulation process is performed for all UEAs and therefore may be a contributing factor in many reports of PPX-C damage *in vivo* [29], [30], [43], [71]. Schmidt *et al.* noted PPX-C damage on iridium microwires which were deinsulated by exposure to a heated element or high-voltage arcing [31], [72]. In these cases, exposure of PPX-C to extreme heat in oxygen containing environments may have resulted in degradation to the parylene films and facilitated subsequent *in vivo* damage.

The evaluation of deinsulation effects on PPX-C was not a primary focus of this study, thus our non-deinsulated and deinsulated reference sample sizes were small. Due to the nature of sample preparation, EDS, XPS and FTIR analyses were performed on

different individual deinsulation samples, and variability in measured oxidation was found between modalities and samples. This variability may reflect variability in the deinsulation process itself, and may play a role in the different damage modes of RAA-processed UEAs. PPX-C film nonuniformity at the micro and macro scale may also play a role, requiring further study of PPX-C characteristics across substrate area, substrates within a single run, and substrates from different runs.

RAA testing of UEAs and test structures has definitively brought to light the possible negative effects of the deinsulation process, and further study utilizing larger sample sizes to understand these effects and mitigate them is warranted. Improved plasma systems or alternative techniques such as laser ablation [73] may be able to decrease oxidation during the deinsulation process. Novel neural electrode technologies incorporating PPX-C are constantly in development, and while common characterization techniques such as EIS have been used to assess heat treatment effects on impedance [74], we have not found impedance to be predictive of PPX-C stability during aging. In such cases, additional spectroscopic methods and RAA can provide deeper insight into possible changes to PPX-C chemistry due to high-temperature processing, as well as an indication of PPX-C resilience to aggressive environments encountered *in vivo*.

4.5.4 Aging damage mechanisms

Little is known about the physiological mechanisms that directly contribute to PPX-C damage *in vivo*. However, considerable effort has been made to understand how thermal and photolytic oxidation influence parylene characteristics, and can help elucidate damage mechanisms at play. Thermal oxidation associated with the appearance

of the carbonyl peak between 1701 and 1695 cm^{-1} has been tied to the formation of ester bonds at aliphatic parylene linkages, leading to chain scission upon further reactions with oxygen [37], and film thinning [38]. *In vivo*, ROS produced by the respiratory burst including H_2O_2 as well as the superoxide anion $\bullet O^-$ and highly reactive hydroxyl radical •OH could initiate hydrogen abstraction at the aliphatic linkage, eventually leading to chain scission and thinning by hydrolysis. Embrittlement and reduction of PPX-C tensile strength through oxidation, as noted for thermally oxidized samples, could lead to crack formation as PPX-C swells from fluid absorption [52]. Photolytic cleavage of chlorine has been identified as another pathway whereby radical sites on PPX-C chains can be created, leading to intramolecular phenylation and hydrogen abstraction [63]. The reduced chlorine measured from explanted devices suggests that a similar pathway may have occurred *in vivo*.

The RAA system was designed to mimic the effects of ROS *in vivo*, but as oxygen and chlorine content of RAA UEAs were different from *in vivo* USEAs and not distinguishable from UEAs aged in PBS, it is difficult to infer the *in vitro* mechanism of damage. PPX-C cracking suggested loss of tensile strength due to oxidation followed by swelling, but cracking was nearly absent for UEAs aged in PBS, which showed similar measurements of oxygen content. We observed thinned PPX-C on several UEAs aged with RAA at 87 °C, and it is possible that analysis of the PPX-C lost to solution, such as through ICP-MS, may yield further clues concerning RAA damage mechanisms. Our choice of characterization modalities was based on prior work that identified similarities between polymers aged *in vivo* and using oxidative test beds, particularly using FTIR [75], [76]. Although RAA damage mechanisms still remain unclear, inclusion of

absorption and emission spectroscopic techniques in our study regimen has yielded several novel insights to inform improvements to neural electrode design.

4.5.5 Choice of neural interface characterization modalities

Much work of great value to the field of neural interfaces has been published concerning the characterization of neural implants in the context of *in vitro* and *in vivo* environments. Such characterization has been commonly conducted using electrochemical spectroscopy and electron microscopy [21], [30], [43], [44], [77], chosen for their applicability to neural electrode performance and ease of use. These techniques are effective for evaluating physical changes to materials, as well as indirect investigation of material chemistry changes inasmuch as these changes are reflected in altered impedances. For UEAs with undamaged IrO_x electrode metal, we found impedance reductions correlated with encapsulation damage. These impedance changes were most apparent at different frequencies depending on the extent of PPX-C damage. Mild, severe, and complete PPX-C damage modes were most reflected in impedance changes near 10^5, 10^3, and 1 Hz, respectively, underscoring the value of full-spectrum impedance measurements for electrode characterization. The 10^3 Hz impedance point has been historically used for neural electrode characterization [67], [78], [79] owing to the characteristic frequency of neural action potentials being on the order of 1 kHz, but this single data point does not fully capture the progression of material damage. Agreeing with prior work [21], we affirm the value to neural electrode characterization of capturing impedance data across multiple frequency points.

However, impedance data alone may not fully communicate electrode material

condition, in the case of multiple damage modes with competing impedance effects. Such was the case for explanted devices, which exhibited increased impedance over time attributed to tip metal damage. This increase in impedance masked any reduction to impedance for these devices arising from encapsulation damage, which was considerable. Complementing impedance spectroscopy, electron microscopy was valuable in identifying multiple physical markers of material damage, including degradation of both electrode metal and encapsulation. Additionally, we employed FIB cross-sectioning to probe material condition further, and for the first time found confirming evidence of PPX-C thinning from *in vivo* aging and RAA processing, as well as signs of silicon erosion *in vivo* underneath the IrO_x tip metallization. These findings aid our understanding of the damage modes and the challenges faced by implanted neural electrodes, and underscore the value of microscopy characterization in addition to SEM surface imaging for probing device damage states.

Not surprisingly, pre-aging characterization using SEM and EIS showed no predictive power for the occurrence of device aging damage, and post-aging characterization with these modalities provided very little information concerning the nature of such damage. By utilizing EDS, XPS, and FTIR we found the first clear signs of oxidation *in vivo* as well as *in vitro* for neural electrodes, and identified processing steps which may have an impact on PPX-C robustness. The utilization of these methods in neural electrode characterization will greatly aid informed design of future electrodes to identify and mitigate failure modes, but obstacles such as sample preparation and the potential for damage to the device might limit their use. Of the three utilized characterization techniques, EDS is the simplest to employ and has indeed been used

previously to characterize explanted microwire electrodes [35]. The technique is considered semi-quantitative, and therefore, care must be used in evaluating trends in the data. XPS can be used to complement EDS measurements, but requires extensive time and expertise to operate, as well as creative sample preparation or analysis techniques for devices with considerable topography, such as the UEA. In addition, discrepancies between EDS and XPS such as those we observed between thermally oxidized and oxygen plasma-etched planar references may arise from the surface-sensitive nature of XPS. FTIR is not as surface sensitive and is widely used for characterizing polymer films, but the volume of analyte required for reliable FTIR analysis can restrict its use. Prior work has evaluated PPX-C for neural microelectrode applications utilizing FTIR, but the small size of actual implanted devices limited FTIR characterization to planar monitor samples soaked *in vitro* [19]. However, we found that the volume of parylene removed from a 4x4 UEA was more than sufficient for repeatable ATR-FTIR measurements. Despite the challenges posed, utilization of characterization methods such as these, in addition to electrochemical and electron microscopy techniques, will greatly enhance neural electrode lifetime data and drive improvements to informed electrode design.

4.5.6 Limits to the work and opportunities for improvement

In this work, we have found favorable comparisons between UEAs aged *in vivo* and using RAA. However, the small sample size of the explanted device cohort limits the confidence of our conclusions, and the strength of our comparisons with previous reports of PPX-C aging is weakened by the fact that most electrodes of previous reports were

used in recording applications, while the USEAs of this report were largely used for stimulation. Therefore, the impact of electrode function on PPX-C damage must be addressed in future work, and analyses of more explanted devices is needed to improve knowledge of conditions encountered by neural microelectrodes, and engineer solutions.

Additional characterization methods can also provide more insight into the changes incurred *in vivo* and *in vivo*. While crystallinity and tensile strength have been noted to be affected by oxidation, our characterization techniques were not suited to such measurements. Preliminary work found that differences in PPX-C Young's modulus based on presence or absence of oxidation could be detected using nanoindentation and peak force tapping atomic force microscopy; however, our efforts to apply these modalities to UEAs were unsuccessful. Through the use of additional methods such as these, material damage mechanisms may be better elucidated.

The RAA system was designed as a test bed that subjects devices to a presumed worst-case scenario *in vivo* incorporating ROS constituents. Such systems have been previously investigated for testing polymers, *e.g.* environmental stress cracking of polyurethanes. Meijs *et al.* found effects similar to *in vivo* stress cracking when polymers were exposed to H_2O_2 at 100 °C [80]. Zhao *et al.* found similar SEM and FTIR characteristics between devices aged *in vivo* and *in vitro* when the *in vitro* system included exposure to H_2O_2 in addition to blood plasma proteins [75] or cobalt chloride [76]. The latter system was designed to produce the •OH through Fenton chemistry, known to occur *in vivo* as part of the respiratory burst [81]. The production of •OH through interactions between H_2O_2 and iron cations has also been associated with parylene cracking in physiological electrolyte at room temperature [82]. These studies

present the possibility of modifying the RAA system to include additional reactants known to drive oxidation processes, with which improved neural electrode devices and material choices can be evaluated.

4.6 Conclusion

In order for neural microelectrodes to be a clinically viable technology, material damage from chronic exposure to the physiological environment must be mitigated. This requires understanding damage mechanisms and having suitable test protocols for evaluating potential solutions, but knowledge in these areas is lacking for neural microelectrode interface technologies. Mechanisms and solutions are specific to the type of material and its function, and in this work we chose to better understand the damage mechanisms of PPX-C, a widely-used and well-regarded dielectric insulating film for neural interfaces. Prior work has shown evidence of PPX-C damage from *in vivo* exposure using SEM and EIS [28], [31], [44], [77], but these modalities did not provide information concerning chemical changes that may point to damage mechanisms and potential solutions.

In the present work, we have developed methods to analyze PPX-C film chemistry on explanted UEAs using absorption and emission spectroscopy techniques, and found evidence of film oxidation and chlorine abstraction for these films. We replicated aspects of *in vivo* PPX-C degradation through oxidative RAA, the first reported time such damage has been recreated *in vitro* for neural interfaces. However, while UEAs aged *in vitro* showed signs of oxidation compared to unaged UEAs, overall PPX-C film chemistry for devices aged *in vitro* was significantly different from devices

aged *in vivo*. Nevertheless, using RAA, oxygen plasma processing of UEAs was identified as a potential cause underlying PPX-C damage *in vitro* and even *in vivo*, underscoring the value of such testing for identifying possible material failure modes. In this sense RAA, is superior to typically employed *in vitro* aging systems comprised solely of buffered saline solution at physiological temperatures or higher, which historically have not uncovered device failure modes prior to costly *in vivo* application and testing. There is a clear need, however, for further work to better understand material aging mechanisms *in vivo*, and how such mechanisms may be simulated in an accelerated fashion *in vitro*.

Future work to meet this need must include more in depth study of devices explanted after chronic *in vivo* use, including chemical spectroscopy modalities such as those used here. The sample size of two explanted USEAs employed in this work was sufficient to demonstrate the value of new characterization techniques and compare RAA outcomes, but general conclusions regarding *in vivo* aging cannot be made with confidence using such a small sample set. As these devices were implanted in peripheral nerve and used for stimulation, differences in material aging may exist with devices implanted in cortex and used for recording. Further work must also incorporate careful material characterization prior to implantation/aging to place post-aging characterization in context, as illustrated by our finding with regard to PPX-C on deinsulated UEAs.

Building on work done using the RAA system, many opportunities exist to further develop *in vitro* aging techniques, such as incorporating acidic species to further mimic the immunological response. As previously mentioned, stimulating neural electrodes may undergo different damage modes from recording electrodes, giving value to test methods

which combine stimulation with soak testing. Importantly, better understanding of activation energies for materials and test methods is needed to confer greater accuracy to equivalent durations of accelerated aging. Common practice is to assume a doubling of aging rate for every 10 °C increase in aging temperature [12], but we found that RAA at 67 and 87 °C caused different damage modes, despite adjusting aging time according to this relationship. This suggests that the current assumptions for accelerated aging are not suitable for all situations without proper justification, and future development of such tests should include studies of reaction kinetics to provide such justification. Through such testing and analysis, data-driven design of medical devices and material choices will facilitate improved outcomes and clinical adoption of novel technologies to improve patient quality of life.

4.7 References

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CHAPTER 5

CONCLUSION

Neuroprosthetics are a promising technology that have demonstrated benefit for those living with paralysis and limb loss [1]–[4], and have the potential to improve the lives of millions of patients [5]. Neural microelectrodes, which permit intimate communication between electronics and neural tissue, are an integral component of this technology, but the limited functional lifetimes of microelectrodes have not allowed novel neuroprosthetics to be translated from research to the clinical space [6], [7]. One factor that contributes to limited microelectrode lifetimes is the failure of dielectric encapsulation materials, which results in reduction of electrode impedance and shunting of charge away from target tissue, and the loss of device performance [8]–[13]. In this work, we successfully evaluated three independent but interrelated strategies for improving the encapsulation performance. Our results demonstrate that through improved testing of dielectric materials, novel application of material properties, and greater understanding of physiological degradation modes, the long-term outlook of implanted neural arrays can be improved.

5.1 Summary of major findings

We investigated three approaches to improve the lifetime for the dielectric encapsulation, the first of which was to develop novel encapsulation materials resilient against dielectric failure modes, such as fluid ingress. We investigated the use of atomic layer deposited aluminum oxide (ALD-Al_2O_3) in combination with parylene C as a bilayer encapsulation strategy. Prior work demonstrated improved encapsulation lifetime for planar test structures, and a very small population of neural electrodes [14]–[16]. In the presented work, we developed new test structures to incorporated the more complex features and topography of actual microelectrodes of the Utah Electrode Array (UEA), and compared test structure results to those of actual UEAs. We statistically quantified the lifetime of the test structures to evaluate the effects of topography on the new encapsulation compared to parylene-only controls. We found that test structures with complex topography and bilayer encapsulation failed at similar or higher rates than parylene controls, with parylene significantly ($p<0.05$) out-performing bilayer encapsulation for fully encapsulated UEAs according to the log-rank test, contrasting with prior work that did not incorporate statistical analysis. We determined that encapsulating film performance can be greatly affected by device topography such as openings in the dielectric film to expose electrode sites. This was evidenced by test structures that incorporated encapsulation openings to simulate these features, which failed more than 10× faster than other test structures, likely due to penetration of phosphate buffered saline (PBS) along the substrate-encapsulation interface. We monitored the time course of impedance reduction for failed devices to better understand failure mechanisms, and found that failed control devices showed rapid (<1 week)

impedance reduction. In contrast, failure of bilayer-coated devices was accompanied by gradual reduction over time (>2 months) to final values more than 10× lower than failed control counterparts. These phenomena were observed through impedance analyses of both test structures and functional UEAs, and were attributed to the etching of ALD-Al_2O_3 layer through parylene defects, leading to undercutting and defect growth over time. These results showed that a key drawback to utilizing ALD-Al_2O_3 as encapsulation for implantable electrodes is its vulnerability to being etched when directly exposed to water. Our results emphasized the need for water-insoluble dielectric materials, and demonstrated the value of our robust testing framework for evaluating materials to be used on neural arrays. This work was published in *Journal of Neural Engineering* [17], with related preliminary work published in *18th International Conference on Solid-State Sensors, Actuators and Microsystems* proceedings [18].

Our second approach investigated how impedance reduction due to encapsulation degradation on neural electrodes can be mitigated by using highly doped *p*-type silicon, a conductive material with high electrochemical impedance when immersed in saline electrolyte. We analyzed how silicon, iridium oxide (IrO_x), and encapsulation contribute to overall UEA impedance spectra, and built a knowledge library of impedances for each material that enables more accurate diagnosis of neural electrode material condition by way of impedance spectroscopy. We also determined that decreasing the coverage of IrO_x on silicon shanks (thereby reducing IrO_x surface area underneath dielectric encapsulation and increasing the same for silicon) would likely improve electrode impedance stability, attributed to the finding that silicon impedance is >100× that of IrO_x deposited on electrode tips. We developed a finite element model that predicted that dielectric damage

that increased silicon exposure to the external environment would have little effect on impedance at frequencies up to 1 kHz, if IrO_x surface area was unchanged. Reactive accelerated aging (RAA), involving the addition of H_2O_2 to PBS to represent oxidative materials degradation mechanisms, was used to compare impedance changes in standard practice UEAs (~300 µm of IrOx below parylene encapsulation) to UEAs with precise IrOx that extended only 20 µm below the edge of the parylene deinsulation. RAA-induced parylene damage caused impedance to be reduced by an order of magnitude at frequencies <1 kHz for standard UEAs, while little change was seen for precise UEAs. Even through insufficient sample size prevented the finding of significant difference between the two populations ($p=0.06$ at 10 Hz), this design approach can very likely improve neural electrode stability and performance *in vivo*. Silicon impedance was found to be more than 10× higher than that of other conductor materials (*e.g.* Pt, Au) used in neural microelectrodes, including carbon fibers with resistivity nearly identical to silicon [19], [20]. This high impedance was considered to arise from a small space charge capacitance within silicon due to physics of the semiconductor-electrolyte interface [21], [22], and may be exhibited by other semiconductor materials. This work identified simple and sound methods to improve UEA stability, and introduced a novel approach to material selection for neural electrode design and fabrication. This work has been published in *Journal of Neuroscience Methods* [23].

The third approach of this work investigated degradation mechanisms for long-term implanted microelectrodes, and evaluated if the RAA test better represents these mechanism, compared to simple PBS immersion lifetime tests. The latter component was strongly motivated by the observation that aging samples in PBS solution was not

representative of degradation observed from samples explanted after long-term implantation. Using electron microscopy, we directly compared RAA aging of UEAs to devices implanted *in vivo* for >3 years, and observed similar instances of parylene C thinning, cracking, and damage between these groups, while devices aged in PBS alone showed little to no parylene C damage. Through absorption and emission spectroscopy, we detected significantly higher ($p<0.01$) oxidation levels for parylene C aged *in vivo* compared to RAA-aged, PBS-aged, and unaged films. This indicates that oxidation-resistant encapsulation strategies may improve long-term device outcomes, and implies that, despite physical damage similarities, RAA may not fully model *in vivo* damage modes. However, artificially aged UEAs did exhibit significantly higher oxidation (regardless of H_2O_2 exposure) than unaged films and films aged on test structures, suggesting that *in vitro* aging at elevated temperatures may capture a component of *in vivo* aging mechanisms. Importantly, we found that degradation incurred during RAA testing of parylene C was correlated with UEA processing in oxygen plasma to remove parylene C at electrode tips, and oxygen plasma processing also corresponded to increased parylene C oxidation compared to unprocessed UEAs. This emphasizes the need to better understand how manufacturing processes impact device performance, and encourages the investigation of alternative processing strategies. Despite finding different film chemistries for UEAs aged *in vivo* and using RAA, our results underscore the value of the RAA system in uncovering potential damage modes, and encourage the use of spectroscopic techniques beyond EIS to better identify material failure mechanisms and corrective actions. This work is currently under preparation for submission to *Biomaterials*.

5.2 Impact and future work

The work presented herein represents the most comprehensive efforts to date to characterize neural electrode material performance. Standard practice in the current literature is commonly limited to broad categorical assessment of materials based on general results (*i.e.* impedance increase or decrease over time, or evidence of damage through electron microscopy, for example see [10], [12], [13], [24]–[26]). Value is often assigned to electrode materials based on these trends, without more detailed analysis of underlying mechanisms. We have employed multiple testing, modeling, and analysis techniques to supplement broad conclusions with deeper insight into mechanisms behind performance. Knowledge of these mechanisms will better inform future material and design choices to enhance long-term neural electrode performance. Just as important, this work highlights methods for robust experimental design and analysis, to improve the testing of future devices and the quality of conclusions drawn from such tests.

5.2.1 Robust encapsulation and conductive materials

Although we found the dissolution of ALD Al_2O_3 to be a likely contributing factor to the failure of Al_2O_3-parylene C bilayer encapsulation, this does not entirely preclude the use of ALD Al_2O_3 for implantable electrodes. Dissolution of this film has been tied to film impurities, which are considered a function of deposition temperature [27]. Therefore, ALD Al_2O_3 deposited at higher temperatures may be suitably robust for implantable applications. Accordingly, work is underway to evaluate the lifetime of ALD AL_2O_3 films deposited at 300 °C, compared to 120 °C deposition temperature used in this work. Based on knowledge gained here, appropriate sample sizes can be chosen (N=20

minimum) to attain statistical significance when testing differences between encapsulations. We are also currently part of a collaboration with researchers at UT Dallas to evaluate low-temperature CVD silicon carbide as an encapsulating dielectric for UEAs. Our collaborators have interest in utilizing fully encapsulated UEAs to evaluate film stability, motivated by the testing resolution these devices offered in our studies.

Work by others is ongoing regarding the development robust materials that can both conduct and insulate. Recently, researchers have fabricated and tested boron-doped nanocrystalline diamond electrodes for neural electrode applications [28], and a just-accepted manuscript from UC Berkeley has reported fabrication of conductive silicon carbide electrodes for the same purpose [29]. These technologies convey the possibilities of fabricating neural interfaces utilizing a single material for both conductor and insulator, eliminating delamination risks normally present for deposited thin dielectric films [30]–[32]. The renowned robustness of diamond and silicon carbide also holds great promise that devices made from these materials will withstand the *in vivo* environment to a degree that previous devices have not. Doped silicon carbide electrodes were also noted to have impedances too high to be useable without Pt electrode film to improve charge transfer between electronics and the *in vitro*/*in vivo* environment [29], similar to our findings concerning conductive silicon. Therefore, these newer materials may be inherently resilient against shunt path formation through dielectric barriers. A comparison between conductive silicon, silicon carbide, diamond, and other similar materials would be highly valuable in determining the material best suited as a neural interface conductor. Both *in vitro* and *in vivo* tests would be required to evaluate the risk of material changes *in vivo*, such as etching, which could change surface roughness and

affect impedance [33].

5.2.2 Improved design of the Utah Electrode Array

Although the UEA has undergone considerable development and use since its introduction two decades ago, this work highlights additional opportunities for its improved design, with applicability to neural arrays in general. These include the optimization of IrO_x tip length (as described in Chapter 3), as well as developing new device architectures utilizing conductive silicon. Given promising results from studies of carbon fiber electrodes [19], [20], a new low-profile UEA may be developed using a combination of deep-reactive-ion etching (DRIE) and other techniques to generate silicon shanks of similar diameter to carbon fibers. Concerns of silicon shank resistance [34] can be alleviated by employing 0.001-0.005 Ω cm silicon, which conductivity is within the same range as reported carbon fibers, and such UEAs would be more readily batch-fabricated than carbon fiber-based devices. However, care would be needed to remove silicon shank surface roughness that would likely arise from DRIE, as local roughness can serve as a fracture nucleation site, increasing silicon brittleness, reducing stiffness, and make protecting the Si surface from dissolution much more difficult.

An additional question to answer regarding UEA performance concerns how manufacturing processes affect end product stability. We found that the UEA plasma deinsulation process may incur changes to the parylene C encapsulation that can render it vulnerable to physical damage in oxidizing aqueous solution, an environment that may be present at the implant site due to the immune response [35]. Therefore, studies are needed of how the plasma deinsulation process affects the parylene that remains on the UEA.

This requires careful characterization of the plasma deinsulation conditions, particularly temperature within the chamber. Temperature characterization can then be used to create a control test involving parylene exposure to similar temperatures without plasma, with and without oxygen, to determine if film oxidation may arise from such conditions. If plasma conditions are widely variable or determined to cause residual film damage, other processes for parylene C removal may be considered, such as use of laser ablation [36].

5.2.3 Better understanding of parylene C aging damage and film quality

Parylene C damage observed through RAA and *in vivo* aging in this work was consistent with prior *in vivo* work with implanted neural electrodes [10], [24], [37], [38]. However, this is at odds with characterization of parylene C exposed to integrated circuit (IC) fabrication procedures, which found that wet etching had little effect on parylene C, including etching in a solution comprised of sulfuric acid and hydrogen peroxide [39]. Also problematic is the lack of pre-aging characterization of parylene C for the mentioned *in vivo* studies, and the finding of one study that did characterize encapsulation prior to neural electrode implantation and identified cracks already present on parylene C films [13]. Therefore, it is not entirely clear from prior literature that damage to parylene C films is solely due to *in vivo* conditions, and future work must be careful to implement identical device characterization (as much as possible) both before and after device aging to support strong conclusions regarding material changes.

This work utilized electron microscopy before and after RAA aging of UEAs, and did find distinct physical damage correlated to oxidative aging conditions. However, this damage varied widely between devices aged simultaneously, and was generally more

severe than damage seen in prior published work. Utah Slanted Electrode Arrays (USEAs) aged *in vivo* also showed severe aging damage, however the pre-implant condition of these devices is unknown. More must be done to understand the cause and mechanisms of material damage, and such work must begin with a sound understanding of parylene C initial conditions. Already mentioned is the need to identify material changes incurred through manufacturing processes, such as oxygen plasma exposure. At a more basic level, the quality and repeatability of the as-deposited film must be properly characterized, to determine if the damage observed here arose from processing defects specific to the deposition system or substrate, or if they reflect general weaknesses in parylene C chemistry.

Parylene C has been generally described in literature as a conformal and pinhole-free film; however, this is not entirely accurate. Film thickness is known to vary across substrates within a given deposition chamber, attributed to small local differences in pressure and temperature [40]. The high aspect ratio of UEA topography may cause local pressure heterogeneity, and we have observed parylene C film thickness on UEAs vary by +80% from target thickness between parylene C at the UEA base and electrode tips. We have also observed pinhole formation on carefully cleaned and prepared planar substrates. Therefore, dedicated experiments are needed to understand parylene C thickness and quality across UEAs within and between batches. At a minimum, such an experimental design may consist of three runs of three UEAs each, with characterization of film thickness through electron microscopy of sectioned and polished UEAs. The prevalence of pinholes can be found by coating large planar electrodes and measuring impedance in saline. Adhesion has also been noted to play a large role in film

performance [30], [32], and while a thorough discussion of parylene C adhesion was not presented here due to it having been addressed in prior work [41]–[43], adhesion across batches must also be tracked for quality control purposes.

Future work may make use of sophisticated spectroscopy techniques, such as imaging spectroscopy modalities, to achieve more detailed analysis of parylene condition and aging. Spectroscopy in this work was largely conducted across large areas to improve signal collection, therefore spatially-specific chemical information within the imaging field was not available. Through imaging spectroscopy, a sample can be scanned by a focused beam source to generate sample images that convey the location of different chemistries within an imaging field. Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) as well as XPS are both surface sensitive spectroscopic techniques that can be operated in an imaging mode, with achievable spatial resolutions of 50 nm and 5 μm, respectively [44]. In the case of cracked parylene on UEAs that exposes underlying silicon, imaging spectroscopy using these methods would readily identify the location of such cracking by resolving regions of exposed silicon on parylene C-coated devices. Imaging ToF-SIMS has also been used to spatially resolve differences in surface oxides for organic electronics [45], which suggests that the same technique may be used to detect local oxidation defects on parylene C-coated devices. This has value for both post-aging analysis as well as pre-aging inspection of parylene C as-deposited or post-deinsulation. Both ToF-SIMS and XPS have been used to analyze changes to fluorinated parylene underneath inorganic capping layers after exposure to oxygen plasma [46]. A similar analysis may be undertaken regarding deinsulation, which exposes parylene C underneath aluminum foil to oxygen plasma.

However, UEA samples must be carefully prepared in order to apply imaging ToF-SIMS and XPS. Preliminary analysis of degraded parylene C on UEAs for the work reported in Chapter 4 included both imaging XPS as well as ToF-SIMS, but these methods did not yield satisfactory results. Experts at NESAC/BIO, a renowned characterization facility, were unable to obtain useable data from UEAs owing to signal scattering from the high aspect ratio UEA topography. Likewise, internal efforts to employ imaging XPS were ruled ineffective due to UEA topography and low levels of captured signal. These attempts preceded the development of UEA sample preparation techniques that presented a more planar sample for analysis, illustrated in Figure 4.1. Future efforts to include imaging XPS and ToF-SIMS characterization may find more success by incorporating these sample preparation techniques.

The work reported herein did not address the mechanical properties of aged parylene C, presenting another opportunity for future work. Mechanical characterization, *e.g.* through peak force tapping atomic force microscopy (PF-AFM) or nanoindention, can detect changes in Young's modulus from aging. PF-AFM is able to resolve highly localized differences in film stiffness, and may shed new light on the characteristics of as-deposited and processed films. Preliminary work to characterize parylene C utilizing PF-AFM (not shown) found evidence of local modulus heterogeneity. In other words, on a sub-micrometer scale, the Young's modulus of parylene C was nonuniform, and seemed to display a bimodal distribution of high and low values. This might reflect localized differences in film density, which may play a role in film degradation for aged devices. For example, lower density regions may degrade more quickly, contributing to the roughened parylene C topography seen for devices aged *in vivo* and through RAA.

There is a clear opportunity for further work in this area, which may influence how parylene C is deposited on implantable devices, or if sufficient disadvantages are found, motivate the use of other films such as crosslinked parylene X, or oxidation- and heat-resistant parylene HT.

5.2.4 Improved *in vitro* models for accelerated aging

Further refinement of the RAA method itself to accommodate more *in vivo* aging mechanisms is another opportunity for future work. Prior groups have developed oxidative systems that replicated *in vivo* damage to polymers by including exposure to blood plasma products [47], or •OH hydroxyl radicals through Fenton chemistry [48]. These groups observed similarities not only through physical inspection, but also in FTIR and chromatography analyses. Additionally, the only known account of parylene crack formation from *in vitro* aging was attributed to Fenton chemistry [49]. Therefore, modifications to the RAA system to include metal cations and induce Fenton chemistry may yield both physical and chemical changes more similar to *in vivo* aging than the current system.

5.2.5 Better understanding and diagnosis of stimulating electrodes

All *in vitro* testing reported in this work has been passive, without the added material stresses caused by electrical stimulation. Exploration of current stimulation effects during RAA aging would further improve understanding of possible device failure modes. Another important topic requiring further investigation is the relationship between impedance and electrode recording/stimulation performance. Impedance is

commonly taken as a *de facto* measure of electrode quality, but no reports have been made that definitively link impedance characteristics with recording signal quality, or that define an optimal impedance for recording if such exists. Furthermore, current stimulation waveforms are dissimilar from EIS source signals, and EIS measurements may not accurately convey stimulation characteristics. Not reported in this work, our efforts to characterize UEA impedance in Chapter 3 led to a preliminary investigation comparing EIS measurements to current stimulation waveforms. We developed an algorithm that predicted voltage transients based on EIS measurements, and for 50 μA biphasic stimulation pulses, the predicted and actual voltage transients were often similar. By adjusting the algorithm, an impedance frequency response curve analogous to EIS measurements could be calculated using a biphasic current stimulation source signal rather than multiple sinusoidal signals at different frequencies. In this way, an electrochemical frequency response can be measured more quickly than traditional EIS, and the calculated spectra more accurately reports operational characteristics during electrode stimulation. This work has implications for improving the general state of neural electrode characterization technology, and has been submitted in an invention disclosure (U-6305), with a provisional cover sheet application to the US Patent Office forthcoming. Both directly and indirectly, the present work has led to multiple efforts and opportunities to improve neural electrode state-of-the-art and the clinical viability of neuroprosthetics.

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